

INSTITUTO TECNOLÓGICO SUPERIOR DE IRAPUATO



INSTITUTO TECNOLÓGICO
SUPERIOR DE IRAPUATO

ESTUDIOS CON RECONOCIMIENTOS DE VALIDEZ OFICIAL
NÚMERO 11-00065

ANALYSIS AND CONTROL OF A DC-DC CONVERTER BASED ON A BIDIRECTIONAL TOPOLOGY FOR VOLTAGE BALANCING OF A DC LINK

OPCIÓN I: TESIS PROFESIONAL

QUE PARA OBTENER EL GRADO DE:
MAESTRA EN INGENIERÍA

PRESENTA:

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IRAPUATO, GTO.

OCTOBER 2025



Educación
Secretaría de Educación Pública



Instituto Tecnológico Superior de Irapuato
Dirección General
Dirección Académica

Irapuato, Guanajuato, **25/septiembre/2025**

Oficio No. CIPI-015-2025

ASUNTO: Autorización impresión tesis de maestría

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Constancia de aprobación de la tesis

La tesis **Analysis and control of a DC-DC converter based on a bidirectional topology for voltage balancing of a DC link** (Análisis y control de un convertidor CD-CD basado en una topología bidireccional para el balance de un enlace de CD) presentada para obtener el Grado de Maestra en Ingeniería en Electrónica fue elaborada por **Diana Geraldine Castañeda Rubalcaba** y aprobada el **30 de septiembre de 2025** por los suscritos, designados por el Consejo de Posgrado de la Maestría en Electrónica del Instituto Tecnológico Nacional de México/ Instituto Tecnológico Superior de Irapuato.

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Créditos Institucionales

Esta tesis fue elaborada en el Laboratorio de Eléctrica y Electrónica de Potencia del Instituto Tecnológico Superior de Irapuato, bajo la dirección del Dr. José Miguel Sosa Zúñiga y el Dr. Gerardo Vázquez Guzmán.

ACKNOWLEDGMENT

Agradezco a la Secretaría de Ciencia, Humanidades, Tecnología e Innovación (SECIHTI) y al Instituto Tecnológico Superior de Irapuato (ITESI) por el apoyo otorgado para la realización de este proyecto de tesis.

Al director de tesis, Dr. José Miguel Sosa Zúñiga, le reconozco y agradezco la confianza, el conocimiento compartido, la dedicación, el tiempo y el apoyo constante.

Al codirector de tesis, Dr. Gerardo Vázquez Guzmán, le expreso mi gratitud por los consejos, los conocimientos compartidos y la confianza.

Al M. I. J. Sacramento Solórzano, gracias por su orientación y entrega como docente, amigo y consejero, *¡Patrón, gracias!*

A la academia de la Maestría en Ingeniería Electrónica, Dr. José M. Sosa, Dr. Gerardo Vázquez, M. I. J. Sacramento Solórzano, Dr. Adolfo Rafael López, Dr. Mario Alberto Juárez Balderas, M. I. José Juan, Dr. Gilberto Muñoz les agradezco y reconozco su labor como docentes. Gracias por su entrega, paciencia y colaboración a lo largo de estos años de formación académica, *¡gracias por hacer posible lo imposible!*

A mi hermana, Laura Castañeda, gracias por las palabras de aliento. A Regina Valtierra, mi sobrina; a mi hermano, Karol Castañeda; mis padres, Gerardo Castañeda y Laura Rubalcaba, *¡muchas gracias!*

A Isaac Tafoya y Miguel Martínez, gracias por su confianza, amistad, compañerismo y apoyo.

Gracias a todos, sin su apoyo, respaldo y motivación constante, este logro no habría sido posible.

Geraldine Castañeda, Octubre 2025.

RESUMEN

Esta tesis presenta el diseño, análisis e implementación de un esquema de control para un convertidor CD-CD no aislado. El objetivo del convertidor controlado es regular, en un sistema estable de lazo cerrado, la diferencia de voltaje entre dos capacitores del enlace de CD de un inversor asimétrico tipo-T de cinco niveles.

El convertidor se basa en una topología Cuk y consta de dos interruptores de potencia y un inductor. El convertidor se conecta a los capacitores del enlace de CD entre la fuente de voltaje de CD y la topología del inversor. Se presenta el análisis del convertidor no aislado para obtener sus características y parámetros en estado estacionario. Además se obtiene y analiza su modelo promedio para proponer un esquema de control. Este se basa en una estructura de control de dos lazos un lazo externo de voltaje con una acción proporcional-integral que regula la diferencia de voltaje entre los capacitores y un lazo interno de corriente con una acción proporcional basada en el error de corriente del inductor.

El esquema de control se analiza mediante el modelo promedio del convertidor, que verifica la estabilidad del sistema de lazo cerrado mediante el criterio de Routh-Hurwitz. También se presentan análisis del lugar de las raíces para caracterizar el efecto de los parámetros de control en el comportamiento del sistema de lazo cerrado. Mediante este análisis, se obtienen valores para los parámetros del esquema de control que garantizan la estabilidad del sistema en lazo cerrado.

El funcionamiento del convertidor y el controlador se valida numérica y experimentalmente en tres configuraciones diferentes. La primera configuración considera el inversor, sin el convertidor, operando en dos condiciones: funcionamiento normal en lazo abierto y funcionamiento en lazo abierto con una condición de falla emulada mediante la conexión de una resistencia en paralelo con uno de los capacitores del enlace de CD. En la segunda configuración, el convertidor se conecta al enlace de CD del inversor, y tanto el inversor como el convertidor operan en lazo abierto, lo que garantiza que el convertidor mantiene voltajes iguales en los capacitores en estado estacionario. Al igual que en la primera configuración, se evalúa el funcionamiento normal en lazo abierto y el funcionamiento en condiciones de falla en lazo abierto. La condición de falla se emula de la misma manera que en la primera configuración. En la tercera configuración, el inversor opera en lazo abierto y el convertidor está conectado a su enlace de CD, pero este último opera en lazo cerrado con el esquema de control propuesto. Al igual que en las configuraciones anteriores, se evalúa el funcionamiento normal y el funcionamiento bajo la condición de falla mencionada.

Se implementó un sistema prototipo de laboratorio para obtener los resultados experimentales. Este sistema incluye circuitos de detección de voltaje y corriente, una tarjeta de interfaz que permite la activación de los convertidores de potencia mediante fibra óp-

tica, y prototipos del convertidor y del inversor multinivel. El control en tiempo real del convertidor se implementa usando un DSP TMS320F28379D. El inversor opera en lazo abierto mediante modulación SPWM implementada en una tarjeta FPGA Altera Cyclone IV.

Los resultados obtenidos muestran que el convertidor de lazo cerrado garantiza la regulación de las voltajes de los capacitores del enlace de CD del inversor a referencias constantes, incluso en caso de falla. El sistema de lazo cerrado presenta un tiempo de respuesta mejorado en comparación con el inversor con enlace de CD sin regulación, o con el convertidor conectado y operando en lazo abierto. El sistema de circuito cerrado propuesto, que consiste del convertidor y su controlador, permite el balance eficaz de los voltajes del enlace de CD de un inversor multinivel, lo que garantiza una regulación del voltaje y un mejor desempeño general del sistema.

ABSTRACT

This thesis presents the design, study, and laboratory implementation of a control scheme for a non-isolated DC-DC converter. The objective of the controlled converter is to regulate, within a stable closed-loop system, the voltage difference between the two capacitors of a DC link of a five-level asymmetric T-type inverter. The converter is based on a Cuk topology and consists of one inductor and two power switches. The converter is connected to the DC link capacitors between the DC voltage source and the inverter topology.

The converter analysis is conducted to determine its steady-state characteristics and parameters. An average state-space model is derived and used to propose a control structure. This control consists of two loops: an outer voltage loop with proportional-integral action to regulate the voltage difference between the capacitors, and an inner current loop with proportional action based on the inductor current error.

The control scheme is analyzed using the converter average state-space model to verify the stability of the closed-loop system through the Routh-Hurwitz criterion. Root locus analysis is also presented to characterize the impact of control parameters on the dynamic behavior of the closed-loop system. From this analysis, appropriate values for the controller parameters are obtained to ensure closed-loop stability.

The performance of the converter and the controller is evaluated and validated both, numerically and experimentally in three different configurations. The first configuration considers the inverter operating in open loop under two conditions: normal operation, and a fault condition emulated by connecting a resistor in parallel with one of the DC-link capacitors. In the second configuration, the converter is connected to the inverter DC-link, and both devices operate in open loop, demonstrating that the converter balances capacitor voltages in steady state. As in the first configuration, both normal and fault conditions are evaluated. The fault condition is emulated as previously described.

In the third configuration, the inverter operates in open loop while the converter is connected to the DC-link and operates in closed loop using the proposed control strategy. Normal and fault conditions are also evaluated as in the previous cases.

An experimental prototype was built to carry out the experimental validation. The system includes voltage and current sensing circuits, an interface board for optically driving the power converters, and hardware prototypes of the converter and the inverter. Real-time control of the converter is implemented using a TMS320F28379D digital signal processor. The inverter operates in open loop with SPWM modulation generated by an Altera Cyclone IV FPGA board.

The results demonstrate that the closed-loop converter successfully regulates the voltages across the DC-link capacitors of the inverter to constant reference values, even under fault conditions. The closed-loop system provides an improved response time in comparison

with an inverter that has an unregulated DC-link, or a converter operating in open loop. The proposed closed-loop system, composed of the converter and its controller, enables effective voltage balancing in the DC-link of a inverter, ensuring proper voltage regulation and improved overall system performance.

Résumé

Cette thèse présente la conception, l'analyse et la mise en œuvre d'un schéma de commande pour un convertisseur DC-DC non isolé. L'objectif du convertisseur DC-DC commandé est de réguler, dans un système stable en boucle fermée, la différence de tension entre deux condensateurs du bus DC d'un onduleur asymétrique en T à cinq niveaux. Le convertisseur repose sur une topologie Cuk et se compose de deux interrupteurs de puissance et d'une inductance. Le convertisseur DC-DC est connecté aux condensateurs du bus DC entre la source de tension continue et la topologie de l'onduleur.

L'analyse du convertisseur DC-DC non isolé est présentée afin d'obtenir ses caractéristiques et paramètres en régime permanent. Un modèle moyen est également dérivé et analysé pour proposer une structure de commande. Celle-ci est basée sur une architecture à deux boucles : une boucle externe de tension, avec une action proportionnelle-intégrale, qui régule la différence de tension entre les condensateurs, et une boucle interne de courant, avec une action proportionnelle basée sur l'erreur de courant dans l'inductance.

Le schéma de commande est analysé à l'aide du modèle moyen du convertisseur, ce qui permet de vérifier la stabilité du système en boucle fermée au moyen du critère de Routh-Hurwitz. Une étude du lieu des racines est également présentée pour caractériser l'effet des paramètres de commande sur le comportement dynamique du système en boucle fermée. Cette analyse permet d'obtenir des valeurs des gains de commande garantissant la stabilité du système.

Le fonctionnement du convertisseur et de la commande est validé numériquement et expérimentalement dans trois configurations différentes. La première configuration considère uniquement l'onduleur, sans le convertisseur DC-DC, fonctionnant en boucle ouverte dans deux conditions : un régime normal, puis un régime de défaut émulé par la connexion d'une résistance en parallèle avec l'un des condensateurs du bus DC. Dans la deuxième configuration, le convertisseur DC-DC est connecté au bus DC de l'onduleur, et les deux convertisseurs fonctionnent en boucle ouverte. Cette configuration permet de montrer que le convertisseur DC-DC assure une égalisation des tensions des condensateurs à l'état stationnaire. Comme dans la première configuration, les conditions normales et de défaut sont évaluées. La condition de défaut est reproduite de la même manière.

Dans la troisième configuration, l'onduleur fonctionne toujours en boucle ouverte, tandis que le convertisseur DC-DC est connecté au bus DC et opère cette fois en boucle fermée avec le schéma de commande proposé. Les mêmes scénarios de fonctionnement normal et de défaut sont analysés.

Un banc de test en laboratoire a été développé pour valider expérimentalement le système. Il comprend des circuits de mesure de tension et de courant, une carte d'interface permettant le pilotage des convertisseurs de puissance par fibre optique, ainsi que les pro-

totypes du convertisseur DC-DC et de l'onduleur multiniveau. La commande en temps réel du convertisseur DC-DC est réalisée à l'aide d'un DSP TMS320F28379D. L'onduleur fonctionne en boucle ouverte avec une modulation SPWM générée par une carte FPGA Altera Cyclone IV.

Les résultats obtenus montrent que le fonctionnement en boucle fermée du convertisseur garantit la régulation des tensions des condensateurs du bus DC, même en cas de défaut. Le système présente un temps de réponse amélioré par rapport à l'onduleur sans régulation ou au convertisseur DC-DC en boucle ouverte.

Le système proposé, composé du convertisseur DC-DC et de sa commande, permet un équilibrage efficace des tensions du bus DC d'un onduleur multiniveau, assurant ainsi une régulation stable de la tension et une meilleure performance globale du système.

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Index of Symbols & Abbreviations

$\wedge$ Conjunction: AND

$\vee$ Disjunction: OR

$\neg$ Negation: NOT

5L-ATT Five-Level Asymmetrical T-Type Inverter

ADC Analog to Digital Converter

DSP Digital Signal Processor

EMI Electromagnetic Interference Effects

EV Electric Vehicles

FC Flying Capacitor Inverter

HRES Hybrid Renewable Energy Sources

HV-DC High-Voltage DC bus

LS-PD-PWM Level-Shifted PWM with Phase Disposition

LUTs Look-Up Tables

Op-Amp Operational Amplifiers

P Proportional

PI Proportional-Integral

PID Proportional-Integral-Derivative

PV Photovoltaic system

PWM Pulse Width Modulation

RES Renewable Energy Sources

SEPIC Single-Ended Primary-Inductor Converter

V2G Vehicle To Grid

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Chapter 1

Introduction

1.1 Converters and their Applications

DC-DC converters are key components in both conventional and emerging applications ranging from basic power regulation in consumer devices to energy management in electric vehicles and renewable energy systems.

The development of major international environmental agreements, such as the Kyoto Protocol, which entered into force in 1997; the Paris Agreement; and the United Nations Sustainable Development Goals, which came into effect in 2015, has accelerated the global energy transition toward clean energy sources and electric mobility. In these contexts, the use of DC-DC converters is important in battery management and renewable energy integration.

As a result, the study, design, and implementation of novel DC-DC converter topologies remain widespread explored in the specialized literature to achieve high efficiency in clean energy generation. This chapter focuses on the review of converters without galvanic isolation, considering both unidirectional and bidirectional topologies, and their application in electric vehicles and renewable energy sources. Special attention is given to the use of DC-DC converters for balancing capacitor voltages in DC links used in some of those applications.

1.1.1 Electric Vehicles

In Electric Vehicles (EV) the use of DC-DC converters is elemental in three parts of the energy management such as; EV chargers, the charging stations and the powertrain.

Electric Vehicles Chargers Types

EV charging methods are generally classified into two categories: wireless charging and conductive charging. Wireless chargers transfer power through magnetic field couplers, eliminating the connectors. This offers high operational flexibility, and typically does not require an on-board DC-DC converter [5]. In contrast, conductive chargers have a galvanic connection between the power supply and the EV connector. This method requires the use of an AC-DC converter and a DC-DC converter to properly regulate the power delivered to the battery. Within conductive charging systems, two architectures are commonly implemented: on-board and off-board chargers.

The charging levels are defined by various international standards applied across different regions. In North America and parts of the Pacific region, the SAE J1772 standard is commonly used. In China, the GB/T 20234 standard governs the EV charging infrastructure, while Europe has adopted the IEC 62196 standard. The difference among these standards lies in how they classify the charging modes: both SAE J1772 and GB/T 20234 categorize them according to the type of power transfer, i.e, AC or DC, whereas IEC 62196 follows a different approach, classifying them according to the connection

method and communication protocols [4, 6].

Table 1.1 presents a comparison of the Level 1, Level 2 and Level 3 charging levels defined in the SAE J1772, IEC 62196, and GB/T 20234 standards. For a more comprehensive analysis, readers may refer to [4–6].

The chargers installed inside EVs are called on-board chargers, and provide the ability to charge the EV directly from the AC grid. Normally, these chargers have a modular structure that includes an EMI filter, a power factor correction converter, an isolated DC-DC converter, and the battery storage. The power factor correction converters are used to enable controllable DC voltage and ensure the harmonic requirements of the grid. The isolated converter guarantees galvanic isolation and manages the power transferred to the battery [7, 8]. In some technical texts, on-board chargers are considered a component of the EV powertrain. In contrast, the off-board chargers can be considered as refueling charging stations, since this charger type is installed outside the EVs. According to SAE J1772 and IEC 62196, on-board chargers typically operate in Level 1 and Level 2 charging, i.e., they involve AC power supplied directly to the vehicle. In contrast, Level 3 charging and extreme fast charging refer to DC fast charging, which is handled exclusively by off-board chargers [4, 7].

Table 1.1: Charging levels defined by international standards [4].

Details	Level 1	Level 2	Level 3	Extreme fast charging
Power (kW)	1.44–1.9	3.1–19.2	20–350	>350
Charger Type	On-board	On-board	Off-board	Off-board
Charging Time	≈20 hours, slow charging	≈5 hours, semi-fast charging	≈30 min, fast charging	≈5 min, ultra-fast charging
Power Supply	12–16 A, 120/230 V _{AC} , Single phase	12–80 A, 208 or 240 V _{AC} , Single/Split phase	, 250–500 A, 208/240 V _{AC} , 300–800 V _{DC} , Three phase	>1000 V _{DC} , 400 A, Higher Polyphase
Standards	IEC 62196, SAE J1772, and GB/T 20234-2		IEC 62196-3	IEC 62196

Types of Charging Stations for Electrical Vehicles

EV charging stations are categorized into three types of architectures based on the supply bus: AC bus, DC bus, and hybrid AC/DC bus structures [4,5]. The conventional charging station shown in Fig. 1.1, uses a three-phase AC bus and includes a transformer between the grid side and the AC bus to ensure galvanic isolation. This transformer also performs a grid voltage step-down to provide an appropriate voltage to the common AC bus. Each EV charging point integrates an AC-DC rectifier followed by a DC-DC converter. The rectifier converts the AC power from the bus into DC, while the converter regulates the output voltage and current to match the battery requirements, enabling safe and efficient charging. However, this architecture increases system complexity, costs, and reduces overall efficiency.

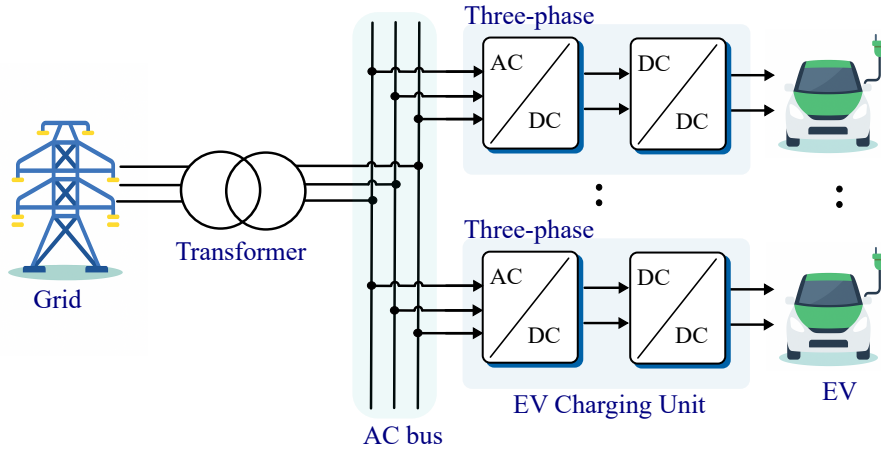


Figure 1.1: The conventional AC bus architecture of a charging station for EV.

DC bus architectures simplify the power conversion path by using a single centralized inverter at the grid interface to supply the DC bus, and a dedicated DC-DC converter at each EV charging point. Figure 1.2 shows this DC bus architecture. These converters are responsible for adapting the bus voltage to the battery charging profile and enable features such as fast charging. The use of converters in this configuration enhances charging efficiency, dynamic response, and allows direct integration of power storage unit and sources of energy renewable through the DC bus. Additionally, bidirectional power flow is possible for Vehicle-To-Grid (V2G) operations with the use of a bidirectional DC-DC converter [4].

The AC/DC hybrid bus structure integrates the AC power grid and various DC sources, such as renewable energy or power storage units. This structure connects the AC and DC buses using individual converters, as shown in Fig. 1.3. Therefore, the AC/DC hybrid bus structure allows simultaneous operation of AC or DC power generation and DC charging, avoiding additional power conversion stages.

The AC and DC buses are interconnected through an inverter, commonly referred to as

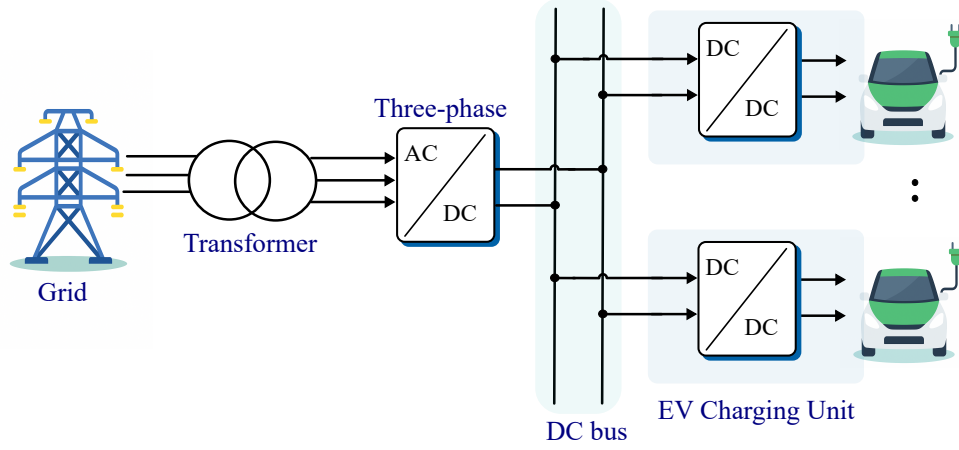


Figure 1.2: The conventional DC bus architecture of a charging station for EV.

an interlinked power converter, enabling flexible integration of both AC and DC loads. The inverter also ensures energy balance between the two buses and operates dynamically based on load requirements. A key element in this architecture is the bidirectional DC-DC converter, which facilitates power flow and enables the implementation of V2G functionality. Its role is essential in optimizing energy flow and supporting high-power DC applications on the DC bus [4].

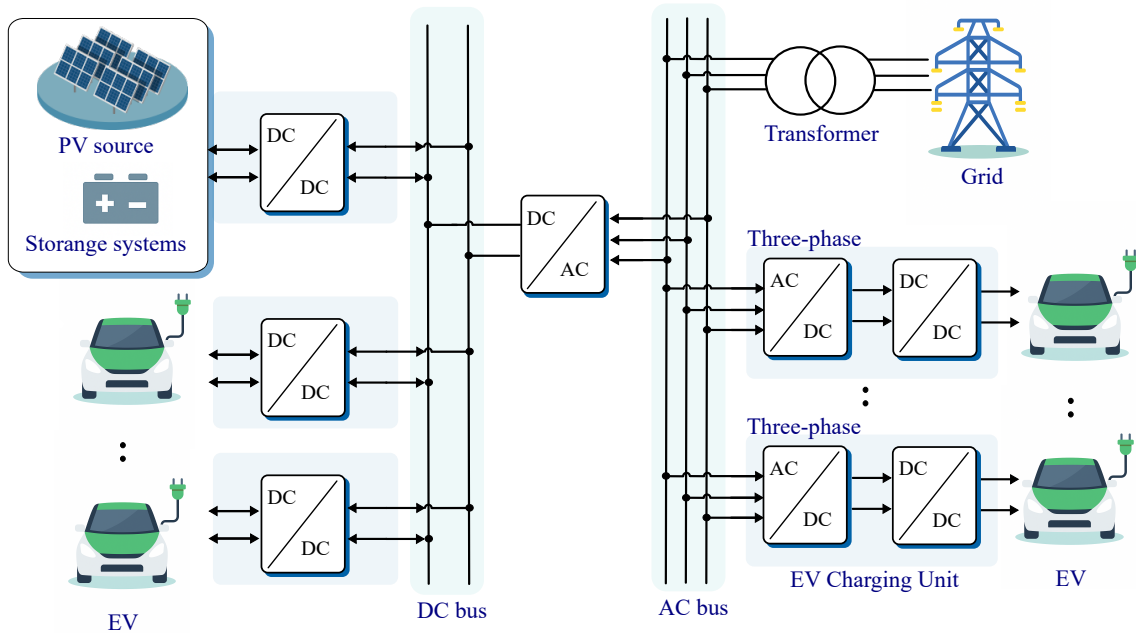


Figure 1.3: The conventional hybrid AC/DC bus architecture of a charging station for EV.

Powertrain of Electrical Vehicles

The powertrain of the EVs is responsible for converting and transferring electrical energy from storage including batteries and supercapacitors to the electric motor, thereby en-

abling vehicle propulsion [9]. This system includes the motor, the battery and DC-DC converters that regulate and adapt the voltage levels according to the vehicle requirements. Figure 1.4 shows a common powertrain structure for a fast-charging station. It includes the connection of the battery and the supercapacitors to High-Voltage DC (HV-DC) bus through individual DC-DC converters [5]. Additionally, this system includes the capability to charge the batteries by using on-board and off-board chargers.

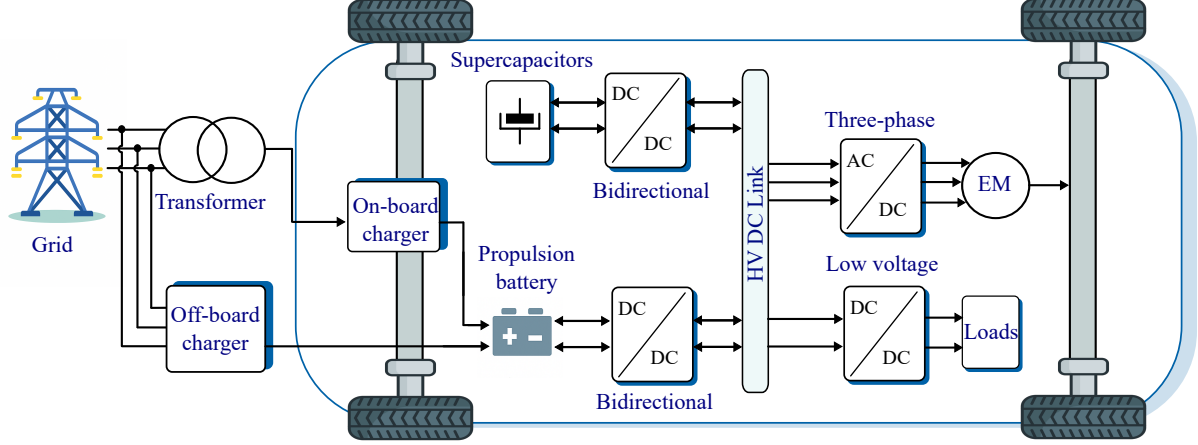


Figure 1.4: Block diagram of an EV powertrain for fast charge.

The HV-DC bus typically operates in the range of 400 V to 750 V [4, 5, 9], providing the voltage required to power the three-phase electric motor, which is the principal load of the system. Since the voltage at the battery terminals is fixed at 250–360 V, which is generally insufficient to directly supply the motor, boost DC-DC converters are used to increase the voltage to the appropriate level of the HV-DC link. Once the required voltage is reached, an inverter converts the energy into variable frequency three-phase AC power, enabling regulation of motor speed and torque. Although using high-voltage transformers to raise the output AC voltage from the inverter could be considered, DC-DC converters are preferred due to their key advantages, such as higher efficiency, smaller size, lower weight, and better cost-effectiveness. These characteristics make DC-DC converters the ideal solution for both EV and hybrid electric vehicles [4, 5, 9].

1.1.2 Sources of Renewable Energy

Sources of renewable energy (RES) systems are composed of integrated power electronics subsystems that enable the efficient conversion and control of energy generated by RES such as photovoltaic (PV) systems, wind turbines, and fuel cells. Typically, a RES includes renewable energy generators, AC-DC or DC-DC power electronic converters, control schemes, loads, or energy storage systems. In RES based on photovoltaic and wind turbines, maximum power point tracking algorithms are implemented to optimize energy harvesting under dynamic environmental conditions. In any RES, DC-DC converters are the most critical component, as they stabilize the output voltage during intermittent

conditions and are more efficient than conventional techniques such as voltage divider circuits using rheostats. Additionally, the integration of non-isolated DC-DC converters allows for reduced system size and lower electromagnetic interference [10,11].

Hybrid Renewable Energy Sources (HRES) integrate multiple renewable energy generation systems. This is a more complex and emerging approach to renewable energy generation, because individual RES are not sufficient to operate as a global power generation system, due to their intermittent nature. Figure 1.5 shows an HRES system that includes the input power generation based on PV source, wind turbines, and fuel cells. Each source features DC-DC converters while the load consists of DC microgrids, AC loads, and DC loads such as charging stations of EV.

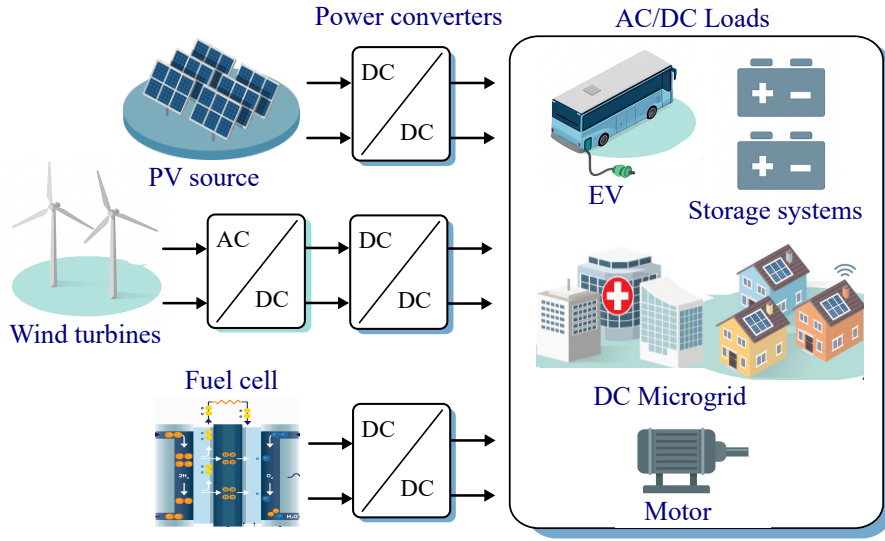


Figure 1.5: DC-DC converter in an HERS structure.

On the other hand, Fig. 1.6 shows an HRES system featuring a DC-DC converter with multiple voltage ports. This configuration allows the entire structure to be considered as a single converter, combining multiple DC or AC sources, with power regulation managed by dedicated controllers. In both systems, it is possible to change the converter by a bidirectional topology to allow energy to flow from sources and to the load or in opposite manner [10, 11]. Some DC-DC converters with multiple voltage ports are reviewed in subsection 2.1.2 of the next Chapter.

1.1.3 Balance of Voltages in DC-link Capacitors

In subsection 1.1.1 and subsection 1.1.2, the architectures of charging stations, power-trains, and chargers for EVs and RES are reviewed, with a focus on the role of converters. In these applications, DC-DC converters are primarily used to regulate the output voltage, enabling high voltage conversion ratios and improved efficiency.

However, in this subsection, converters are reviewed for balancing the voltage across DC-link capacitors in systems such as RES, DC microgrids, and multilevel inverters [12–20].

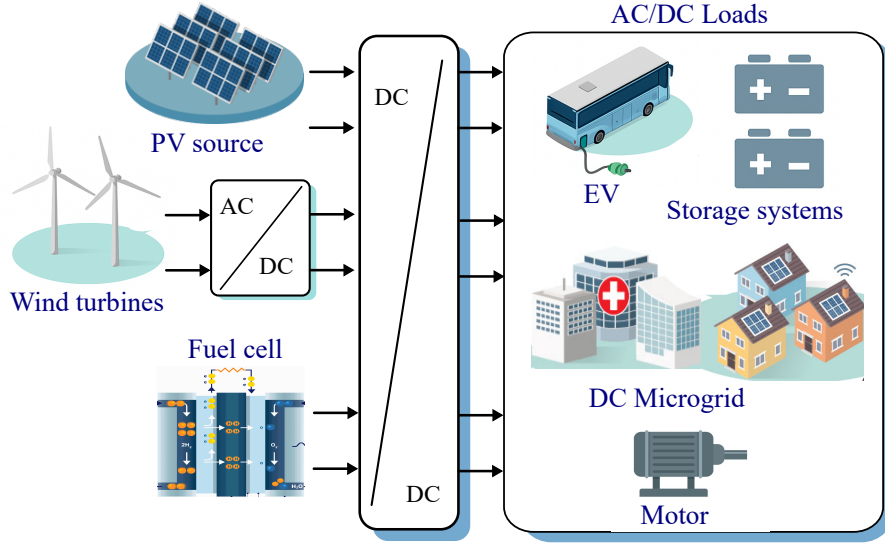


Figure 1.6: DC-DC converter with a multiple voltage ports in an HERS structure.

Voltage unbalance in DC-link capacitors can arise from different causes depending on the application. In DC microgrids, it often results from asymmetrical power distribution between the capacitors, which occurs when the connected loads draw unequal currents. This voltage unbalance causes one capacitor to charge or discharge faster than the other, leading to unequal voltage levels.

In multilevel inverters, the unbalance voltage in DC-link capacitors is an inherent problem of the topology or the modulation scheme used, i.e. in the Neutral Point Clamped (NPC) inverters the neutral point is inherently unbalanced [21]. This results in both a DC offset and AC ripple at the neutral point, leading to a constant voltage variation between the top and bottom capacitors of the DC link. The voltage unbalance in DC-link capacitors is undesirable because it degrades power quality, increases stress on power switches, and in severe cases, can damage power converters. Several studies propose using DC-DC converters as active balancing circuits to address this issue.

Various topologies and strategies have been presented in which converters are used specifically to balance the voltage across the DC link capacitors. [12–20]. In [16], a typical buck-boost converter is presented for balancing a two-capacitor DC link in a DC microgrid. Additionally, this study is used to propose four active balancing circuits based on Cuk, Super-SEPIC (Single-Ended Primary-Inductor Converter)-Zeta, and interleaved buck-boost converters. Experimental results from a laboratory prototype based on the interleaved buck-boost converter are also included. In [17] a SEPIC-Cuk converter is proposed for RES applications to balance the voltage in a two-capacitor DC link.

In [12] the use of a converter based on the use of buck and boost converters to balance the DC-link voltage of a five-level NPC inverter is presented. Using this same principle, in [19] and [15], converters to balance a DC link in a multilevel inverter are proposed. In [19] a three-level converter is proposed which is implemented in a low-voltage DC

three-phase system. The converter consists of one inductor, a pair of power switches, and two DC link capacitors. Meanwhile, in [15] the converter integrated four freewheeling diodes, four power switches, two DC link capacitors, and a LC filter in the output port. This converter is used in EV charging stations.

In [13] a bidirectional DC-DC converter is proposed to balance the DC link of a DC microgrid. This converter prevents unbalance of the DC link capacitors and enables the power to flow in both directions between the storage system and DC link. It uses two inductors and four power switches. In [12, 18], a boost converter is proposed to balance the DC-link of an NPC inverter in RES applications. This converter consists of one power switch, $(2n_L - 1)$ diodes, one inductor, and capacitors, where n_L corresponds to the total number of voltage levels generated by the NPC inverter.

In [20] a novel buck-boost DC-DC converter, suitable for high-power and medium- to high-voltage applications, is presented. Its main features include low voltage stress on the power switches, low switching losses, and reduced output filter volume. The analysis considers the five-level bidirectional version of the one that operates in buck mode.

1.2 Motivation and Objectives

In the current context of the energy transition, DC-DC converters assume a fundamental role in the efficient and controlled integration of RES, as well as in the development of emerging technologies such as EV and DC microgrids. They are capable of adapting voltage levels, regulating power flow, and enable bidirectional architectures makes them essential components in modern applications that demand efficiency, reliability, and flexibility. Additionally, converters are used in special applications to manage balanced DC link voltages in system with multiples sources.

In this context, the study, analysis, and implementation of a conventional control strategy for a bidirectional converter capable of regulating the voltage unbalance across the DC link capacitors are presented in this thesis. The DC-link under consideration consists of two capacitors and forms part of a five-level asymmetrical T-type inverter. Although several alternative approaches have been presented in the literature [12–20], most of them focus on DC links used in renewable energy systems or DC microgrids. Additionally, many of these converters operate in open-loop mode or implement different control strategies. In contrast, this work focuses on a controlled bidirectional converter integrated into the DC link of a multilevel inverter structure.

General Objective

The general objective of this thesis is to design, analyze, and implement a control scheme for a non-isolated bidirectional DC-DC converter aimed at balancing the capacitor voltages of a DC link.

Specific Objectives

- To analyze and model a non-isolated bidirectional DC-DC converter in order to propose a control scheme to balance voltages in a DC link.
- To perform numerical simulations of the proposed control scheme to validate the closed-loop operation of the bidirectional DC-DC converter.
- To conduct experimental tests under various electrical conditions to validate the operation of the bidirectional DC-DC converter with the implemented control scheme.

1.3 Outline

This thesis is structured in the following six chapters. Chapter 1 is organized into three sections, in which a review of DC-DC converter applications is presented. These sections cover their use in chargers, charging stations, and the powertrain of EV, as well as their role in RES and in balancing voltages across DC-link capacitors. Chapter 2 is organized into two sections. The first one section reviews unidirectional and bidirectional DC-DC converters. The second one section focuses on typical control schemes reported in the literature for these converter topologies. Chapter 3 is also organized into two sections. The first describes the DC-DC converter and its operating principles. The second presents the averaged model, the proposed control strategy, and a closed-loop stability analysis. Chapter 4 is divided into two sections. These sections describe the operating principle and modulation scheme of the five-level asymmetrical T-type inverter. Numerical validation is also included. Chapter 5 presents the design and experimental implementation of the laboratory prototype, along with the experimental results. Finally, Chapter 6 summarizes the conclusions of this thesis.

Chapter 2

Converters without Galvanic Isolation and Control Schemes

In this chapter, the unidirectional and bidirectional converters are reviewed. The chapter consists of two main sections. Section 2.1 presents conventional topologies such as boost, buck-boost, Cuk, and SEPIC, as well as their variants. Additionally, novel bidirectional converter topologies are discussed and categorized into the following subgroups: bidirectional topologies derived from simpler topologies, topologies with multiple voltage ports, topologies employing different voltage levels, converters constructed with half-bridge or full-bridge configuration, and converters featuring soft-switching. Section 2.2 is dedicated to reviewing the typical control schemes reported in the literature for the implementation and design of non-isolated converters. The focus of this section is on control strategies: energy-based control, Proportional-Integral (PI) and Proportional-Integral-Derivative (PID) controllers, sliding mode control, and model predictive control.

2.1 Converters without Galvanic Isolation

Switched-mode DC-DC converters arose beginning with the appearance of semiconductor switches in the 1950s [22]. These converters replaced the use of linear counterparts due to their advantages, such as high efficiency, power density, and low weight. Their first applications were in the aerospace and telecommunications industries [22, 23]. This type of converter is capable of transforming the input DC voltage into an output voltage of either higher or lower magnitude, with the same or opposite polarity, and with or without galvanic isolation between input and output ground references. The output voltage magnitude is regulated through Pulse Width Modulation (PWM).

Switched-mode converters are divided into two main groups: galvanic isolation and without isolation. Isolated topologies first convert the DC voltage into an AC signal, which is transferred through a transformer with high-frequency operation and subsequently rectified back into DC. The inclusion of galvanic isolation allows for a high step-up voltage gain ratio and provides enhanced protection. However, isolated converters are usually larger in size and exhibit higher EMI due to parasitic capacitance in the transformer. In contrast, non-isolated converters avoid the use of galvanic isolation and, therefore, do not suffer from transformer-induced noise, resulting in lower EMI compared to isolated topologies. Additionally, they typically feature simpler configurations, reduced weight, and higher efficiency. Some reported non-isolated topologies even achieve voltage gain ratios comparable to those of isolated converters [24, 25].

Non-isolated topologies can be divided into unidirectional and bidirectional converters. Figure 2.1 presents some of the most commonly used topologies of unidirectional and bidirectional converters. In Table ?? are summarized the efficiency, the control scheme uses, and the application of each topology of Figure 2.1.

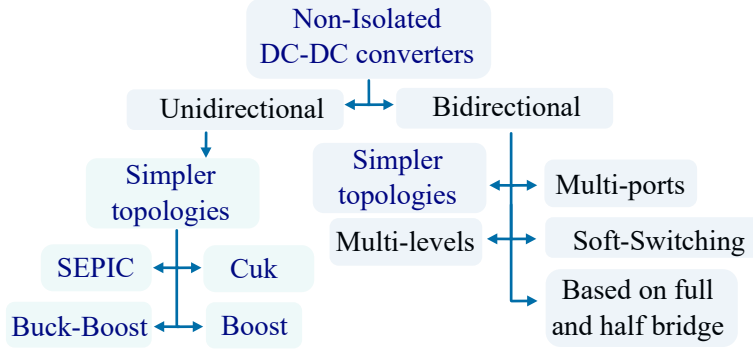


Figure 2.1: Classification of the non-isolated DC-DC converters.

2.1.1 Unidirectional Converters

Unidirectional topologies are characterized by power flow in a single direction; that is, the DC voltage source supplies the DC load. The buck, boost and buck-boost converters [23, 26] are the typical unidirectional topologies, and their operating principle and design lay the groundwork for the study and development of new topologies such as SEPIC, Cuk and other novel topologies reported in the specialized literature. In this subsection, the buck-boost, SEPIC and Cuk DC-DC converters are discussed.

The buck-boost converter is depicted in Fig. 2.2 [23, 26, 27]. This topology unifies the buck and boost converters, allowing the input voltage to be converted into an output voltage of either higher or lower magnitude. It uses a DC voltage source, one power switch, S , a power diode, D , one inductor, one capacitor, and a resistive load. Equations in (2.1) define the voltage gain ratio, as well as the output voltage, ΔV_C , and the current ripple, ΔI_L .

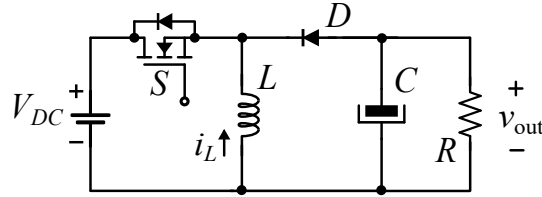


Figure 2.2: Schematic diagram of the buck-boost unidirectional converter.

$$\frac{V_{out}}{V_{DC}} = -\frac{k}{1-k}, \quad \Delta I_L = \frac{V_{DC}k}{Lf_s}, \quad \Delta V_C = \frac{k}{RCf_s}. \quad (2.1)$$

The variable k is the duty cycle of S , f_s denotes the switching frequency, V_{DC} is the input voltage, and L and C are the values of the inductance and capacitance, respectively.

The voltage gain of the Cuk converter is similar to that of the buck-boost converter, that is, it can adjust the output voltage magnitude up or down with a polarity opposite to that of the input. However, this converter is built using a DC voltage source, power switch, S , one power diode, D , a pair of inductors, L_1 and L_2 , and a pair of capacitors, C_1 and C_2 .

The addition of two passive components compared to the buck-boost converter results in lower ripple in both input and output currents due to continuous conduction [23, 26].

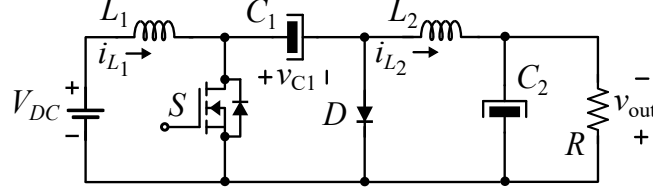


Figure 2.3: Schematic diagram of the Cuk unidirectional converter.

The Cuk converter is shown in Fig. 2.3. The voltage gain, capacitor voltage ripples, ΔV_{C_1} and ΔV_{C_2} , and inductor current ripples, ΔI_{L_1} and ΔI_{L_2} , are described in (2.2)–(2.3),

$$\frac{V_{out}}{V_{DC}} = -\frac{k}{1-k}, \quad \Delta V_{C_1} = \frac{V_{DC}k^2}{2(1-k)RC_1f_s}, \quad \Delta V_{C_2} = \frac{1-k}{8LC_2f_s^2}, \quad (2.2)$$

$$\Delta I_{L_1} = \frac{V_{DC}k}{2L_1f_s}, \quad \Delta I_{L_2} = \frac{V_{DC}k}{2L_2f_s} \quad (2.3)$$

where k is the duty cycle of S , f_s denotes the switching frequency, V_{DC} is the input voltage, capacitance and inductance values are set as C_1 , C_2 , L_1 and L_2 , respectively.

The SEPIC converter uses the same components as the Cuk converter, and provides a similar voltage gain. An important difference lies in the output voltage keeping the same polarity as the input. While the overall topology resembles that of the Cuk converter, the positions of inductor L_2 and the power diode D are rearranged. In the SEPIC converter, one terminal of L_2 is connected to a common reference point, and the other is connected between capacitor C_1 and diode D . On the other hand, D is connected between L_2 and C_2 . In contrast, the Cuk converter connects these elements in the opposite order. This difference in configuration is what causes the SEPIC converter to generate the output voltage and input voltage with the same polarity. Figure 2.4 shows the schematic diagram of the SEPIC converter.

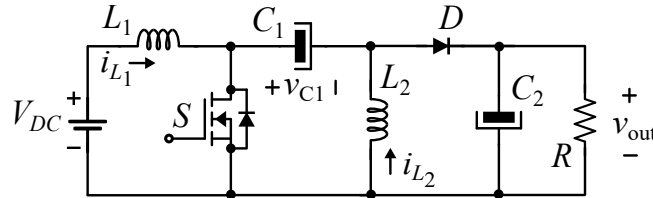


Figure 2.4: Schematic diagram of SEPIC unidirectional converter.

The advantages of the SEPIC converter compared to the buck-boost and Cuk converters are its capability to increase or decrease the output voltage magnitude while maintaining the same polarity as the input, and its continuous input current, which reduces EMI and input filtering requirements. The voltage gain, capacitor voltage ripples, ΔV_{C_1} and ΔV_{C_2} , and inductor current ripples, ΔI_{L_1} and ΔI_{L_2} , of the SEPIC converter are described in

(2.5)–(2.4),

$$\frac{V_{out}}{V_{DC}} = \frac{k}{1-k}, \quad \Delta V_{C_1} = \frac{V_{out}k}{RC_1f_s}, \quad \Delta V_{C_2} = \frac{V_{out}k}{RC_2f_s} \quad (2.4)$$

$$\Delta I_{L_1} = \frac{V_{DC}k}{L_1f_s}, \quad \Delta i_{L_2} = \frac{V_{DC}(1-k)}{L_2f_s} \quad (2.5)$$

where k is the duty cycle of S , f_s denotes the switching frequency, V_{DC} is the input voltage, C_1 C_2 , L_1 and L_2 are the capacitance and inductance values, respectively.

2.1.2 Bidirectional Converters

The operating principle of unidirectional topologies serves as the conceptual basis for bidirectional topologies. However, bidirectional topologies emerge to improve energy flexibility and control, as they enable power flow in both directions. That is, the voltage ports of bidirectional topologies are connected to batteries or systems capable of operating either as a DC loads or as a power supplies [28].

The main bidirectional topologies arise from replacing the unidirectional power switches in buck-boost, Cuk, and SEPIC converters with bidirectional power switches. Additionally, the switching signals of the bidirectional power switches are complementary and synchronous. Figure. 2.5 shows the buck-boost, Cuk, and SEPIC bidirectional topologies.

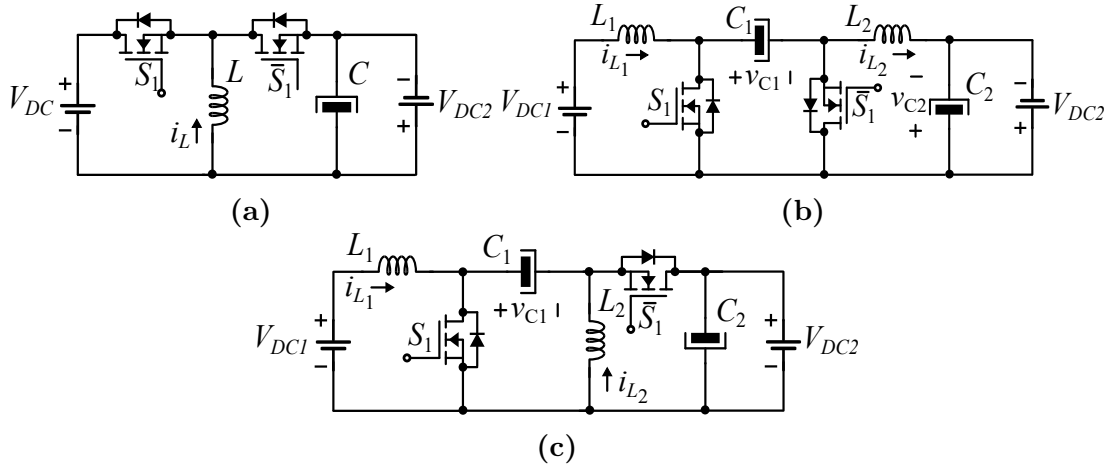


Figure 2.5: Schematic diagram of bidirectional topologies derived from simpler converters. (a) buck-boost, (b) Cuk, and (c) SEPIC converters.

Several novel topologies have been proposed and reported in the specialized literature. This subsection reviews some of these bidirectional topologies, which are classified as follows: bidirectional topologies derived from simpler converters; topologies with multiple voltage ports; bidirectional topologies employing different voltage levels, converter

constructed with half-bridge or full-bridge configuration, and converter featuring soft switching. [29].

In [30–32] bidirectional converters derived from the SEPIC converter, are proposed. In [31], a wide conversion ratio bidirectional SEPIC converter that incorporates a non-dissipative snubber to achieve zero current switching is presented. In [33] three bidirectional converter with high voltage gain range are proposed. These topologies result from the combination of a boost converter with other configurations like Cuk, SEPIC, and buck-boost converters.

The topologies with multiple voltage ports enable the management of multiple DC sources or loads [34]. In [35], the authors introduces a three-port buck-boost converter with high step-up, and step-down ratios, combining buck and buck-boost structures. It includes two unidirectional ports and one bidirectional port, and the topology is used for battery integration in PV systems. In [1] a four-port non-isolated converter for EVs, capable of buck, boost, and buck-boost outputs, is proposed. The schematic diagram is shown in Fig. 2.6. It features five operation modes to handle different combinations of inputs and outputs. Regenerative braking energy is stored via bidirectional paths, while auxiliary systems are powered uni-directionally. Additionally, a three-input converter with four independent switches for hybrid systems is presented in [36].

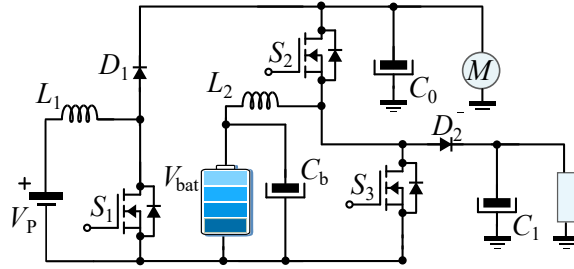


Figure 2.6: Schematic diagram of the converter proposed in [1].

These topologies are essential in applications such as hybrid electric vehicles, since the output voltage must adapt to voltage ports with different levels of magnitudes voltage. In [2] a three-level converter with application on EVs using batteries and ultracapacitors is proposed. This topology is shown in Fig. 2.7. In [37] a four-level flying-capacitor converter is introduced, that interfaces batteries with the DC bus in HEVs. It reduces inductance requirements and supports variable input-output voltage ratios. In [38] a three-level bidirectional converter with improved dynamic response due to a smaller inductor, is presented.

These topologies typically use dual half-bridge configurations, either voltage-fed or current-fed [39, 40]. Some topologies are integrated with buck-boost converters or modular architectures. They are capable of achieving high DC voltage conversion ratios in different modes, including buck, boost, and buck-boost modes. In [39] a family of the bidirectional converters without galvanic isolation and with high DC gain is presented, based on

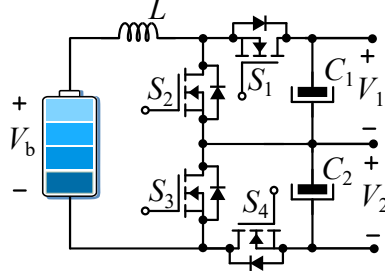


Figure 2.7: Schematic diagram of the topology proposed in [2].

a dual half-bridge topology with a magnetically coupled split inductor. These converters support buck, boost, and buck-boost operating modes. In [40] a non-isolated boost bidirectional converter with bidirectional fault-blocking is proposed for medium/high-voltage grids. It features grid-side buffer subcircuits and lower component count. A dual-active half bridge integrated into a buck-boost topology, shown in the Fig. 2.8, that enhances voltage gain and allows soft switching is proposed in [3].

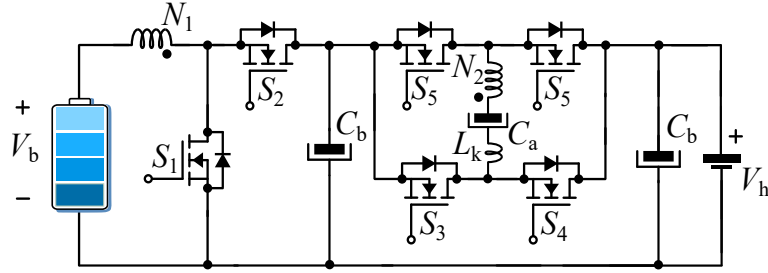


Figure 2.8: Schematic diagram of the topology proposed in [3].

The main feature of these topologies is the use of the zero voltage switching or zero current switching techniques to decrease switching losses, increase efficiency, and lower EMI. Some topologies add resonant branches, auxiliary inductors and capacitors, or coupled inductors to enable soft switching [41]. In [42] a soft-switching bidirectional converter family without auxiliary switches is proposed. Those converters use a small inductor and capacitors. One advantage of these topologies is the reduced ripples; the drawbacks are high switch currents and inductor core loss. In [43] a coupled-inductor bidirectional converter that enables ZVS in both directions, with stress reduction and efficiency improvement, is presented.

2.2 Typical Control Schemes

In applications such as PV systems, EVs, RES, and battery energy storage systems, control schemes are essential for the operation of DC-DC converters, which are responsible for adapting voltage levels, managing power flow, and ensuring reliable energy conversion between various system components.

The integration of control schemes into these applications is essential to ensure the regula-

tion of output voltage or current. Moreover, control schemes guarantee that the converter meets the desired operating conditions despite disturbances such as load variations, input voltage fluctuations, or dynamic environmental conditions. Control schemes also optimize energy efficiency, reduce switching losses, and enhance system stability, particularly during transient events such as startup, shutdown, or sudden load changes.

In addition, control systems manage the energy flow between sources and storage elements, such as in EV powertrains ensuring proper charging, discharging, and power distribution. These operating conditions are typically encountered in systems that employ bidirectional converters. Control schemes also contribute to maintaining safety, preventing overvoltage or overcurrent conditions, and minimizing EMI problems generated during switching. Overall, control systems are essential to guarantee the performance, robustness, and reliability of DC-DC converters in emerged energy applications. In this subsection the energy based control, the PID and PI control schemes, the sliding mode control and the Model Predictive Control (MPC) are briefly mentioned and described without detailed examination [11, 44]. Additionally, in the Table ?? are summarized the different control schemes use DC-DC converters are summarized.

Energy-based techniques have been employed in converter control by using the idea that these systems reach steady state by regulating how energy is dissipated. These controllers shape the energy profile of the converter to improve the transient response and ensure system stability. There are two main types of energy-based control namely, stabilizing control and passivity-based control [44].

The stabilizing control is based on Lyapunov methods. It uses the concept of energy increment to indicate the distance between the converter current operating point and the equilibrium point, which corresponds to the minimum energy state [44]. This energy is commonly defined by the energy stored in the inductor and capacitor elements, as shown in (2.6)

$$\dot{V}(z) = \frac{1}{2} \left(\sum_{x=1}^{n_L} L_x \dot{i}_{L_x}^2(z) + \sum_{y=1}^{n_C} C_y \dot{v}_{C_y}^2(z) \right), \quad (2.6)$$

where L_x represents the individual inductances associated with the n_L inductors, C_y denotes the capacitances of the n_C capacitors, and $\dot{i}_{L_x}$ and $\dot{v}_{C_y}$ are the derivatives of the inductor currents and capacitor voltages, respectively. This formulation ensures that the energy decreases over time toward its minimum value, guaranteeing global stability even under large disturbances.

In [45, 46] a cascaded DC-DC boost converter is proposed for the integration of a hybrid battery system into the power grid with the uses of a stabilizing control. In [47] the proposed controller employs composite switched Lyapunov functions to improve the efficiency and performance of the buck and buck-boost converters.

Passivity-based control is designed to render the converter passive, thereby ensuring its

stabilization by shaping the internally stored energy. A key advantage of this method is that once the converter becomes passive, it retains this property even when arbitrarily interconnected with other passive components within a DC system.

This theoretical property guarantees stable operation and satisfactory performance under a wide range of external disturbances and interactions with other system components. However, a significant limitation of passivity-based control is its reliance on the precision of the converter model, which can reduce the robustness of the controller in the presence of modeling uncertainties [44].

There are two methods to design passivity-based control. In the first one, the converter is represented as an Euler–Lagrange dynamical system that exchanges energy with its environment. The second method, involves port-controlled Hamiltonian models, representing a wide range of nonlinear systems that include Euler–Lagrange models [44]. In [44, 48–50] different passivity-based controls for unidirectional converters are designed and implemented.

The Proportional (P), Proportional-Integral (PI), and Proportional-Integral-Derivative (PID) controllers are classical control strategies commonly applied in the regulation of converters. Inductor currents or capacitor voltages are measured variables that are compared to predefined references, resulting in error signals that are processed by the controller to generate an appropriate control action [44, 51].

The P controller offers a fast dynamic response by adjusting the control signal proportionally to the instantaneous error. However, it cannot fully cancel out the steady-state error, making it more suitable for applications where fast reaction is prioritized over precision, such as inner current loops in converters [51].

The PI controller combines the proportional action with an integral term that collects the error over time, efficiently eliminating steady-state error for step inputs. This makes it particularly well-suited for output voltage regulation in the presence of input voltage fluctuations or load variations common in applications like electric vehicles and photovoltaic systems. Although the PI controller may exhibit a slower transient response and requires careful tuning to avoid oscillations, it provides greater robustness and improved steady-state performance compared to the P controller [51].

The PID controller integrates proportional, integral, and derivative actions to regulate system behavior. Therefore, it combines the individual advantages and limitations of each action. The proportional gain provides a fast dynamic response by acting directly on the control error; however, it cannot eliminate the steady-state error by itself. To address this limitation, the integral gain accumulates the error over time, effectively eliminating the steady-state error, particularly in the presence of external disturbances or abrupt shifts in the reference input. Nevertheless, a pole at the origin is added due to the integral gain, which can negatively affect closed-loop stability if not properly tuned. To mitigate

this effect and enhance the system robustness, the derivative gain is introduced. It is sensitive to the errors rate of change, helping to reduce rapid error variations and improve transient performance. This component is particularly effective in damping oscillations, limiting overshoot, and minimizing the impact of high-frequency disturbances, such as those caused by setpoint changes or measurement noise [51].

In some converter applications, P, PI, and PID control schemes are implemented using two main approaches: single-loop control and double-loop control. Single-loop control relies on a single feedback signal to regulate the behavior of the system. The controller directly modifies the duty cycle of the converter according to the error between the reference signal and the measured output. On the other hand, double-loop control incorporates two nested control loops: an inner loop and an outer loop. This structure enhances dynamic performance and stability.

In [31] a PI current control strategy is proposed to regulate the bidirectional power flow. A double-loop PI control, in which the inner loop regulates the current and the outer loop regulates the voltage, is proposed in [33].

Sliding Mode Control (SMC) is a nonlinear and discontinuous control technique known for its robustness against external disturbances and system uncertainties. Its goal is to drive the system state toward a sliding surface and keep it there to ensure stability. However, it can cause undesired oscillations known as the chattering effect, which is why it is often combined with other techniques to reduce this phenomenon. SMC has broad industrial applications, including EVs, motor control, and renewable energy systems, maintaining the performance of converters under varying load conditions [11, 44, 52].

In [53, 54] a SMC scheme is developed and applied in a buck converter. In [55] a robust voltage regulation method for boost converters using dynamic SMC combined with interval type-2 fuzzy neural networks is proposed. The method models system uncertainties, designs a novel sliding surface, and employs adaptive online learning to handle parameter variations.

Model Predictive Control (MPC) is an advanced control method that predicts the system future behavior using a mathematical model and feedback. It is especially effective for managing multivariable (MIMO) systems, such as multiple DC-DC converters in renewable energy applications. MPC enables efficient regulation and contributes to minimizing operating costs, improving power flow management, and optimizing economic load dispatch. Its implementation enhances the converter response to variations on both the input side and the load side [11, 44, 52, 56].

Chapter 3

Description and Modeling of the Studied Converter

In this chapter, the non-isolated converter studied in this thesis is presented and analyzed, with its application focused on the voltage balance in inverter DC-link capacitors. The content is organized into three sections. In the first section, the derivation of the converter from the conventional Cuk topology is presented, together with its operating principle. In the second section, the converter averaged model is obtained and the proposed control strategy is presented. The control approach follows a two control loop classical structure: the inductor current is regulated by the inner loop using a proportional action, while the voltage balance variable is regulated by the outer loop using a proportional-integral control action i.e. the difference of voltages across the DC-link capacitors.

3.1 Description and Operation Principle

The converter studied in this thesis is based on the bidirectional Cuk converter [52]. Figure 3.1 (a) shows the bidirectional Cuk converter. It consists of two inductors L_1 and L_2 , two capacitors, C_a and C_b , two power switches, S_a and $\bar{S}_a$, and two DC voltage sources defined as V_1 and V_2 . This bidirectional converter can be redrawn as shown in Fig. 3.1 (b), where capacitor C_b is neglected. Additionally, by replacing capacitor C_a with a DC voltage source V_{DC} , V_1 and V_2 with two capacitors denoted as C_1 and C_2 , respectively, and by merging the inductors L_1 and L_2 into one single equivalent inductor denoted as L , the converter studied in this thesis is obtained and depicted in Fig. 3.1 (c).

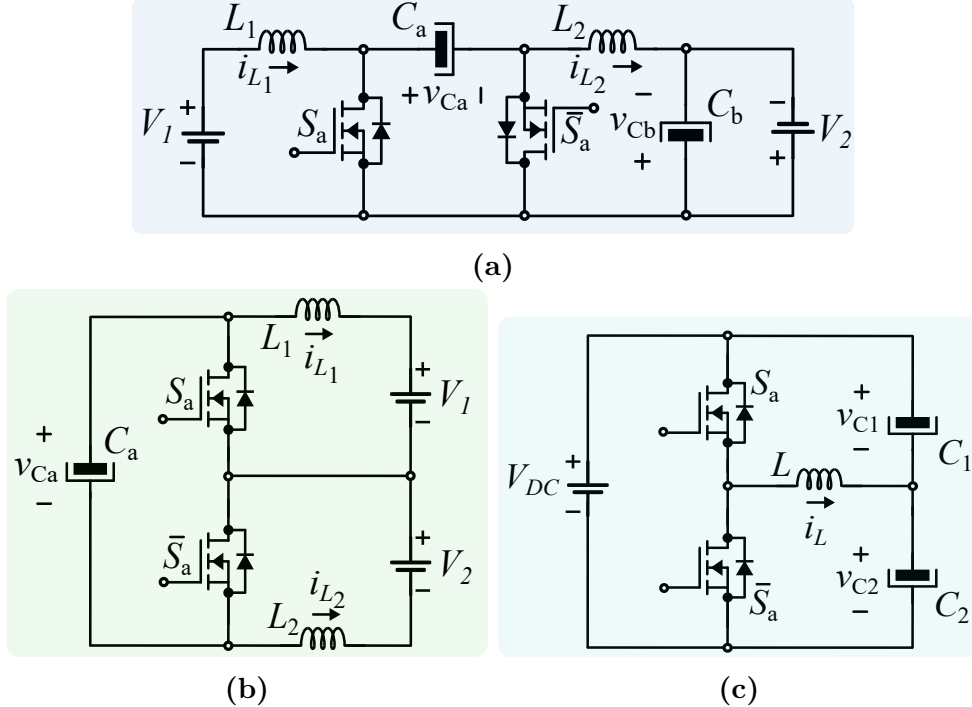


Figure 3.1: Schematic diagram of (a) the bidirectional Cuk converter and its redraws (b) and (c) to obtain the converter studied in this thesis.

The activation of the power switches S_a and $\bar{S}_a$ is driven by two complementary and synchronous switching signals. As a result, the operation of the converter can be described

based on the two states generated by the switching of S_a . If S_a is activated during a time interval denoted as t_1 , the converter operates according to the equivalent circuit shown in Fig. 3.2a. Conversely, if S_a is deactivated during the interval t_2 , the equivalent circuit is as shown in Fig. 3.2b.

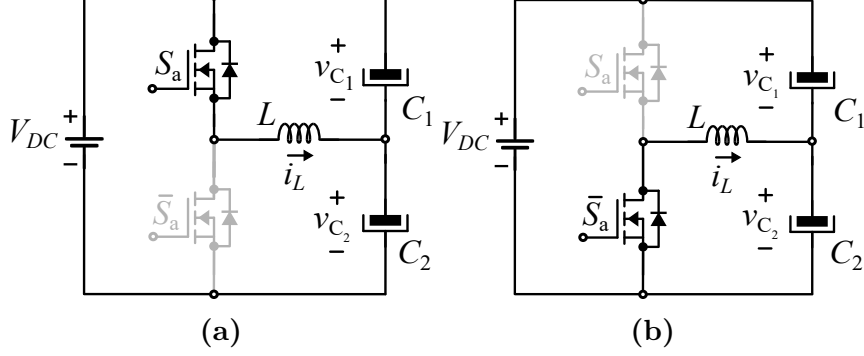


Figure 3.2: Equivalent schematic diagrams for each switching combination. (a) In the time interval $[0, kT_s]$, (b) in the time interval $[kT_s, T_s]$.

The relationship between the time interval t_1 and the switching period, T_s , defined the duty cycle, it expressed by (3.1).

$$k = \frac{t_1}{T_s} = \frac{t_1}{t_1 + t_2}. \quad (3.1)$$

Figure. 3.3 shows the waveform of the duty cycle, and the two intervals of time can be redefined by $t_1 = [0, kT_s]$ and $t_2 = [kT_s, T_s]$.

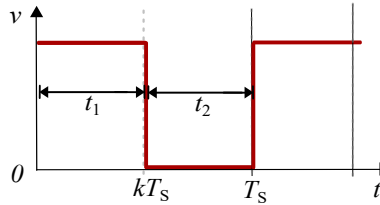


Figure 3.3: Switching signal of S_a during one switching period, T_s , $t_1 = [0, kT_s]$ and $t_2 = [kT_s, T_s]$.

According to the inductor volt-second and the capacitor charge balance, the capacitor voltage $v_{C_i}(t)$, $i = 1, 2$, and the inductor current $i_L(t)$ are composed of a nominal DC voltage component and a small superimposed AC component, and are described by:

$$v_{C_i}(t) = V_{C_i} + v_{ripple}(t), \quad i_L(t) = I_L + i_{ripple}(t), \quad (3.2)$$

the AC component can be neglected by assuming: $|v_{ripple}| \ll V_{C_i}$, and $|i_{ripple}| \ll I_L$, then

$$v_{C_i}(t) \simeq V_{C_i}, \quad i_L(t) \simeq I_L, \quad (3.3)$$

by definition, the voltage of the inductor and the current of the capacitor are given by,

$$v_L(t) = L \frac{di_L}{dt}(t), \quad i_{C_i}(t) = C_i \frac{dv_{C_i}}{dt}(t), \quad (3.4)$$

this behavior can be observed as a linear increment, resulting from the high switching frequency,

$$V_L = L \frac{\Delta I_L}{\Delta t}, \quad I_{C_i} = C_i \frac{\Delta V_{C_i}}{\Delta t}. \quad (3.5)$$

Analyzing the equivalent circuit during the time interval $[0, kT_s]$, the voltage of the inductor, V_L , and the currents of the capacitors, I_{C_1} and I_{C_2} , are given by,

$$V_L = V_{C_1}, \quad I_{C_1} = I_{C_2} - I_L, \quad I_{C_2} = I_{C_1} + I_L. \quad (3.6)$$

Analyzing the equivalent circuit during the time interval $[kT_s, T_s]$, V_L , I_{C_1} , and I_{C_2} are given by,

$$V_L = -V_{C_2}, \quad I_{C_1} = I_{C_2} - I_L, \quad I_{C_2} = I_{C_1} + I_L. \quad (3.7)$$

Using (3.5) and (3.6) and considering that $I_L/2 = I_{C_1} = -I_{C_2}$, the ripple current inductor, ΔI_L , and the ripple voltage capacitors, ΔV_{C_1} and ΔV_{C_2} , are defined by,

$$\Delta I_L = \frac{V_{C_1} k}{f_s 2L}, \quad \Delta V_{C_1} = \frac{V_{C_1} k}{16C_1 L f_s^2}, \quad \Delta V_{C_2} = \frac{V_{C_1} k}{16C_2 L f_s^2}, \quad (3.8)$$

where f_s is the switching frequency defined by $f_s = 1/T_s$. Figure. 3.4 shows the behavior of (3.8).

The converter can be used as a multi-port converter by connecting a DC load in parallel with each capacitor. Therefore, the voltage conversion ratios are defined by,

$$V_{C_1} = (1 - k) \cdot V_{DC}, \quad V_{C_2} = k \cdot V_{DC}, \quad (3.9)$$

where k denotes the duty cycle of switch S_a . A suitable application of this converter is the voltage balancing in two series-connected capacitor DC-link in inverters as presented in Chapter 4.

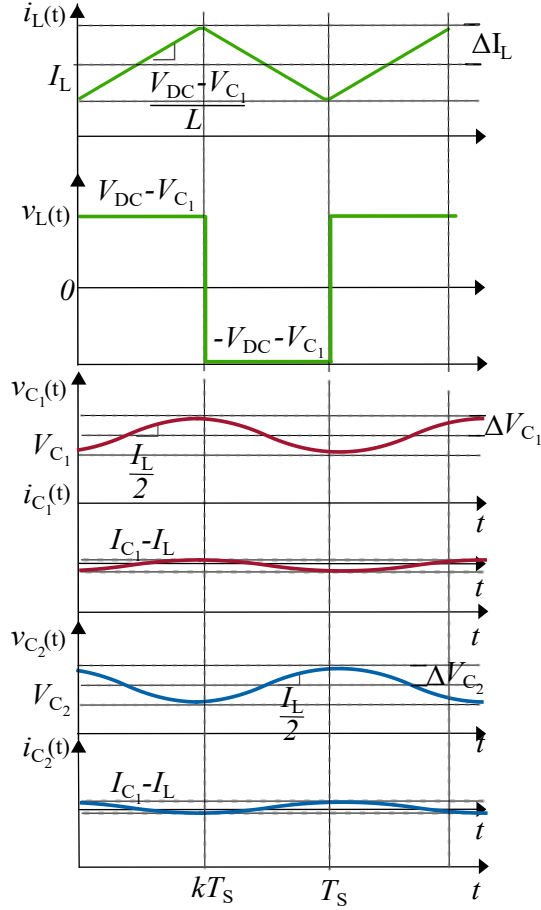


Figure 3.4: Waveforms of the inductor current and voltage capacitors during one switching period, T_s . In descending order, inductor current and voltage, voltage and current across C_1 , and voltage and current across C_2 .

3.2 Averaged Model and Control Proposal

The analysis and modeling of the converter is obtained under the following assumptions: the switching signals of power switches S_a and $\bar{S}_a$ are complementary and synchronous, all circuit elements are considered ideal; thus, parasitic components are neglected. Additionally, two DC current sources, which are assumed of constant values, I_a and I_b , are connected in parallel with the capacitors to model the current demanded by a given load, as shown in the diagram of Fig. 3.5.

The model is obtained by the averaging over a switching period of the two equivalent circuits resulting in one switching period. Those equivalent circuits are shown in Fig. 3.6. Define the state variables which x_1 and x_2 as the voltages across each capacitors, C , and x_3 the current through the inductor, L . Additionally, it is assumed that the capacitance $C_1 = C_2 = C$, the inductance L and the DC voltage V_{DC} are constants. The state space model when the switch S_a is in conduction in the time interval $[0, kT_s]$ is result in (3.10)

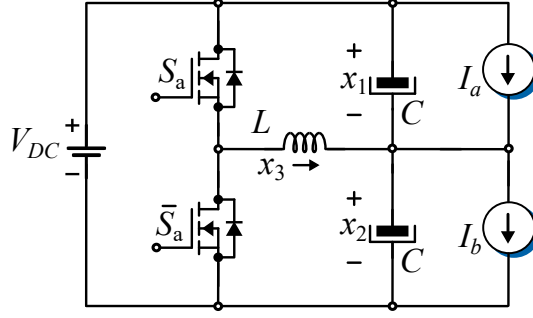


Figure 3.5: Schematic diagram of the converter.

and (3.11).

$$C(\dot{x}_1 - \dot{x}_2) = -x_3 - I_a + I_b \quad (3.10)$$

$$2L\dot{x}_3 = x_1 - x_2 + V_{DC} \quad (3.11)$$

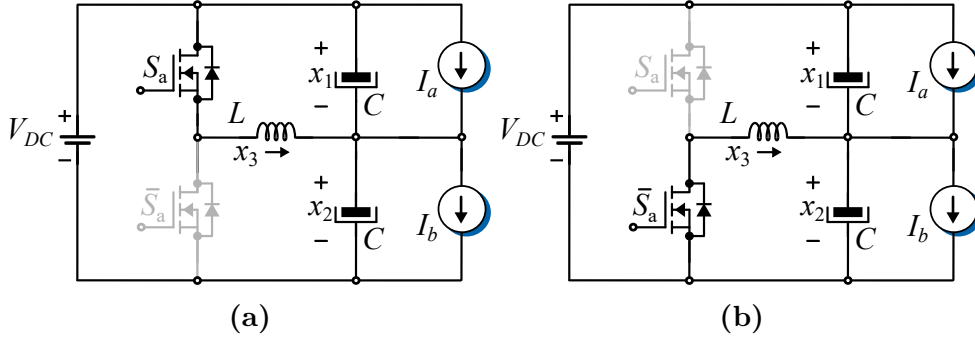


Figure 3.6: Equivalent schematic diagrams for each switching combination. (a) In the time interval $[0, kT_s]$, (b) In the time interval $[kT_s, T_s]$.

Equation (3.11) results from the addition of the expressions $L\dot{x}_3 = -x_2 + V_{DC}$ and $L\dot{x}_3 = x_1$. These two equations represent the dynamic behavior of the inductor current in the equivalent circuit. When the switch S_a is turned off, the state space model is given by equations (3.12) and (3.13).

$$C(\dot{x}_1 - \dot{x}_2) = -x_3 - I_a + I_b \quad (3.12)$$

$$2L\dot{x}_3 = x_1 - x_2 - V_{DC} \quad (3.13)$$

Equation (3.13) results from the addition of the expressions $L\dot{x}_3 = x_1 - V_{DC}$ and $L\dot{x}_3 = -x_2$.

Since V_{DC} is constant, the sum of the capacitor voltages is constant during the two switching combinations, ($\dot{x}_1 + \dot{x}_2 = 0$). Then, the state space model can be redefined using only two state variables $y_1 := x_1 - x_2$ and $y_2 := x_3$. Additionally, $I_b - I_a$ is considered a perturbation and is denoted by $p := I_b - I_a$.

Therefore, the state space models described by (3.14) and (3.13) can be expressed by

(3.14) to (3.15).

$$C\dot{y}_1 = -y_2 + p, \quad 2L\dot{y}_2 = y_1 + V_{DC}, \quad (3.14)$$

$$C\dot{y}_1 = -y_2 + p, \quad 2L\dot{y}_2 = y_1 - V_{DC}, \quad (3.15)$$

Equations (3.14) can be expressed in a matrix form by $Q\dot{y} = A_{t_1}y + B_{t_1}$. Moreover, (3.15) can be expressed in a matrix form by $Q\dot{y} = A_{t_2}y + B_{t_2}$. In both matrix expressions $Q = \text{diag}\{C, 2L\}$ is the 2×2 diagonal matrix that has the passive element values at its main diagonal, A_{t_i} , $i = 1, 2$, represents the state matrices, and B_{t_i} , $i = 1, 2$, represents the state matrices. Then,

$$A_{t_1} = A_{t_2} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, \quad B_{t_1} = \begin{bmatrix} p \\ V_{DC} \end{bmatrix}, \quad B_{t_2} = \begin{bmatrix} p \\ -V_{DC} \end{bmatrix} \quad (3.16)$$

To obtain the state space model that describes the behavior of during a switching period, its necessary to obtain the averaged model by integrating the matrix A_{t_i} , $i = 1, 2$, and B_{t_i} , $i = 1, 2$, from $[0, kT_s]$ to $[kT_s, T_s]$.

$$A_{avg} = \frac{1}{T_s} \int_0^{kT_s} A_{t_1} dt + \frac{1}{T_s} \int_{kT_s}^{T_s} A_{t_2} dt = (A_{t_1} - A_{t_2})k + A_{t_2} \quad (3.17)$$

$$B_{avg} = \frac{1}{T_s} \int_0^{kT_s} B_{t_1} dt + \frac{1}{T_s} \int_{kT_s}^{T_s} B_{t_2} dt = (B_{t_1} - B_{t_2})k + B_{t_2} \quad (3.18)$$

Consequently, the averaged model is given by,

$$C\dot{y}_1 = -y_2 + p, \quad (3.19)$$

$$2L\dot{y}_2 = y_1 + 2V_{DC}u - V_{DC}, \quad (3.20)$$

where the duty cycle of S_a averaged over switching period of the converter is defined by $u \in (0, 1)$. The averages model has the matrix form $Q\dot{y} = A_0y + uB_0 - B_1$, where:

$$A_0 = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, \quad B_0 = \begin{bmatrix} 0 \\ 2V_{DC} \end{bmatrix}, \quad B_1 = \begin{bmatrix} p \\ V_{DC} \end{bmatrix} \quad (3.21)$$

of (3.19)–(3.20) is observed that the system is linear and controllable, subject to a constant perturbation.

The control objective is to regulate the voltage unbalance between the capacitors, that is regulate $y_1 = x_1 - x_2$ toward a constant reference value $y_{1,r}$. If $y_{1,r} = 0$ then each voltage capacitor x_1 or x_2 is regulated to $V_{DC}/2$, else x_1 is regulated to $-(V_{DC} - y_{1,r})/2$, and x_2

to $V_{DC} - y_{1,r}/2$. Control proposed in this thesis incorporates an outer loop to regulates the voltage balance, y_1 , using a proportional-integral gain, and a inner loop to regulated the inductor current, y_2 , using a proportional gain, it is given by;

$$u = -y_2 k_{p_c} + k_{p_v} k_{p_c} (y_1 - y_{1,r}) + k_{p_c} y_3, \quad (3.22)$$

$$\dot{y}_3 = k_{i_v} (y_1 - y_{1,r}), \quad (3.23)$$

where y_3 is an auxiliary state variable resulting from the inclusion of the integral action, k_{p_c} , k_{p_v} y k_{i_v} are controller parameter constants. A block diagram of the proposal control is depicted in Fig. 3.7.

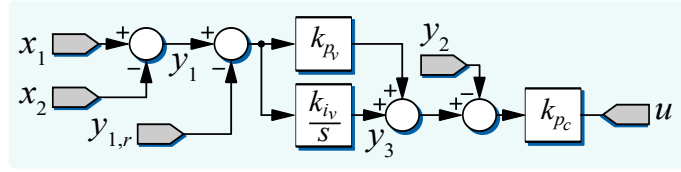


Figure 3.7: Block diagram of the proposed controller.

Considering the averaged model (3.19)–(3.20), and the input control, $u = -y_2 k_{p_c} + k_{p_v} k_{p_c} (y_1 - y_{1,r}) + k_{p_c} y_3$, the state space model in closed-loop is given by (3.24)–(3.26).

$$C\dot{y}_1 = -y_2 + p \quad (3.24)$$

$$2L\dot{y}_2 = y_1 + 2V_{DC}k_{p_c}k_{p_v}(y_1 - y_{1,r}) - 2k_{p_c}V_{DC}y_3 - V_{DC} \quad (3.25)$$

$$\dot{y}_3 = k_{i_v}(y_1 - y_{1,r}) \quad (3.26)$$

The state variables of equilibrium in the closed-loop system are defined by (3.27).

$$y^* = [y_1^*, y_2^*, y_3^*], \quad y^* = \left[y_{1,r}, p, p + \frac{V_{DC} - y_{1,r}}{2V_{DC}k_{p_c}} \right] \quad (3.27)$$

The error variables are defined by $z = y - y^*$, then $z_1 = y_1 - y_1^*$, $z_2 = y_2 - y_2^*$ and $z_3 = y_3 - y_3^*$. Therefore, the error model of the closed-loop system is defined by:

$$C\dot{z}_1 = z_2 - y_2^* \quad (3.28)$$

$$2L\dot{z}_2 = (1 + 2V_{DC}k_{p_c}k_{p_v})(y_1 - y_1^*) - V_{DC}k_{p_c}L(z_2 - y_2^*) - V_{DC}k_{p_c}L(y_3 - y_3^*) \quad (3.29)$$

$$\dot{z}_3 = k_{i_v}(y_1 - y_{1,r}) \quad (3.30)$$

Equations (3.28)–(3.28) can be described in the matrix form by $Q\dot{z} = Az$:

$$\begin{bmatrix} C & 0 & 0 \\ 0 & 2L & 0 \\ 0 & 0 & 1 \end{bmatrix} \dot{z} = \begin{bmatrix} 0 & -1 & 0 \\ (1 + 2V_{DC}k_{p_c}k_{p_v}) & -V_{DC}k_{p_c}L & -V_{DC}k_{p_c}L \\ k_{i_v} & 0 & 0 \end{bmatrix} z \quad (3.31)$$

The characteristic equation polynomial of the closed-loop system (3.24)–(3.26), is given by:

$$\Delta(s) = s^3 + \frac{V_{DC}k_{p_c}}{L}s^2 + \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{2LC}s + \frac{V_{DC}k_{p_c}k_{i_v}}{2LC}. \quad (3.32)$$

To guarantee system stability, all roots of the characteristic polynomial must have negative real parts. This condition can be verified using the Routh-Hurwitz stability criterion. The characteristic polynomial, $\Delta(s)$, is a third-order polynomial of the form:

$$\Delta(s) = a_0s^3 + a_1s^2 + a_2s + a_3, \quad (3.33)$$

where

$$a_0 = 1, \quad a_1 = \frac{V_{DC}k_{p_c}}{L}, \quad a_2 = \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{2LC}, \quad a_3 = \frac{V_{DC}k_{p_c}k_{i_v}}{2LC}. \quad (3.34)$$

The Routh-Hurwitz table for the third-order polynomial is given by:

$$\begin{array}{c|cc} s^3 & a_0 & a_2 \\ s^2 & a_1 & a_3 \\ s^1 & b_1 & 0 \\ s^0 & c_1 & 0 \end{array}$$

where

$$b_1 = \frac{a_1a_2 - a_3}{a_1}, \quad c_1 = \frac{b_1a_3 - a_1b_2}{b_1}, \quad (3.35)$$

substituting the values of the coefficients:

$$\begin{array}{c|cc} s^3 & 1 & \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{2LC} \\ s^2 & \frac{V_{DC}k_{p_c}}{L} & \frac{V_{DC}k_{p_c}k_{i_v}}{2LC} \\ s^1 & \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{L} - k_{i_v} & 0 \\ s^0 & \frac{V_{DC}k_{p_c}k_{i_v}}{2LC} & 0 \end{array}$$

To ensure stability, each element in the first column must have a positive value. Therefore, the following conditions are assumed:

$$1 > 0, \quad \frac{V_{DC}k_{p_c}}{L} > 0, \quad \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{L} - k_{i_v} > 0, \quad \frac{V_{DC}k_{p_c}k_{i_v}}{2LC} > 0, \quad (3.36)$$

under these conditions, it is proposed:

$$k_{p_c}k_{i_v} > 0, \quad k_{i_v} < \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{2L} \quad (3.37)$$

The condition of k_{i_v} depends on the converter parameters, specifically the DC voltage V_{DC} and the inductance L . Nevertheless, there exists a feasible range of controller parameters that guarantees system stability.

To verify the stability the root locus method is used. The roots of the closed-loop characteristics equation are equivalent to the solution of

$$\Delta(s) = s^3 + \frac{V_{DC}k_{p_c}}{L}s^2 + \frac{1 + 2V_{DC}k_{p_c}k_{p_v}}{2LC} + \frac{V_{DC}k_{p_c}k_{i_v}}{2LC} = 0, \quad (3.38)$$

which can be rewritten as:

$$1 + kG(s) = 0, \quad 1 + k_{p_v}G_{k_{p_v}}(s) = 0, \quad 1 + k_{i_v}G_{k_{i_v}}(s) = 0 \quad (3.39)$$

where k_{p_c} , k_{p_v} and k_{i_v} , is the gain under variation in the interval from zero to infinity, and $G_{k_{p_c}}(s)$, $G_{k_{p_v}}(s)$, and, $G_{k_{i_v}}(s)$, are the corresponding equations dependent on this gain. This formulation allows for evaluating the effect of each gain individually while keeping the others constant. Equations (3.40)–(3.42) represent the specific cases of equation (3.39) when the variable gains are k_{p_c} , k_{p_v} , and k_{i_v} , respectively.

$$1 + k_{p_c}G_{k_{p_c}}(s) = 1 + k_{p_c} \left(\frac{\frac{V_{DC}}{L}s^2 + \frac{V_{DC}k_{p_v}}{LC}s + \frac{V_{DC}k_{i_v}}{2LC}}{s^3 + \frac{1}{2LC}s} \right) = 0 \quad (3.40)$$

$$1 + k_{p_v} G_{k_{p_v}}(s) = 1 + k_{p_v} \left(\frac{\frac{V_{DC} k_{p_c}}{LC} s}{s^3 + \frac{V_{DC} k_{p_c}}{L} s^2 + \frac{1}{2LC} s + \frac{V_{DC} k_{p_c} k_{i_v}}{2LC}} \right) = 0 \quad (3.41)$$

$$1 + k_{i_v} G_{k_{i_v}}(s) = 1 + k_{i_v} \left(\frac{\frac{V_{DC} k_{p_c}}{2LC} s}{s^3 + \frac{V_{DC} k_{p_c}}{L} s^2 + \frac{1 + 2V_{DC} k_{p_c} k_{p_v}}{2LC} s} \right) = 0 \quad (3.42)$$

The equation where $G_{k_{p_c}}(s)$, is used (3.40), has three poles located at $\{0, +j\sqrt{\frac{1}{2LC}}, -j\sqrt{\frac{1}{2LC}}\}$, and two zeros, given by:

$$\left\{ \frac{-k_{p_v}/C}{2} \pm \frac{\sqrt{k_{p_v}^2/C^2 - 2k_{i_v}/C}}{2} \right\}. \quad (3.43)$$

The equation where $G_{k_{p_v}}(s)$ has been defined, has a single zero at the origin and three poles given by:

$$\left\{ 0, -\frac{V_{DC} k_{p_c}/L}{2} \pm \frac{\sqrt{(V_{DC} k_{p_c}/L)^2 - 2(1 + 2V_{DC} k_{p_c} k_{p_v})/LC}}{2} \right\}. \quad (3.44)$$

In contrast, $G_{k_{i_v}}(s)$ has a single zero, and one pole at the origin. The remaining poles are the roots of a third-order characteristic equation with real coefficients that can be determined analytically using algebraic methods or numerically evaluated.

Using the parameters shown in Table 3.1 the stability of (3.40)–(3.42) is analyzed using the root locus method. Figure 3.8 shows the root locus of $G_{k_{p_c}}(s)$, which has three poles: two located on the imaginary axis and one at the origin. In addition, all trajectories lie in the left half-plane.

Table 3.1: Parameters of the converter.

Element	Value
V_{DC}	80 V
L	2 mH
C	1000 μ F
k_{pc}	1/4
k_{pv}	$2k_{pc}$
k_{iv}	$1/2k_{pc}$

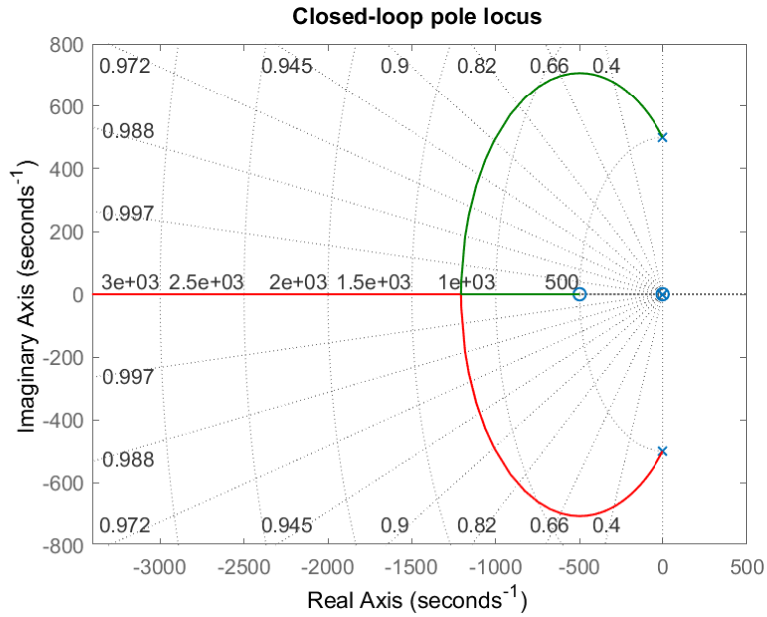


Figure 3.8: Locus of poles and zeros in closed loop of $G_{k_{pc}}(s)$ as $k_{pc} = 1/4, 2k_{pc}=k_{pv}$ and $k_{iv} = 1/2k_{pc}$.

Figure 3.9 shows the root locus of $G_{k_{pv}}(s)$, which has a single zero at the origin and three poles; two of them are complex conjugate, and the remaining one is located at the origin. All branches of the root locus remain in the left half-plane.

Figure 3.10 shows the root locus of $G_{k_{iv}}(s)$, which has a single zero and a pole at the origin and two complex conjugate poles. Again, all root locus trajectories are located

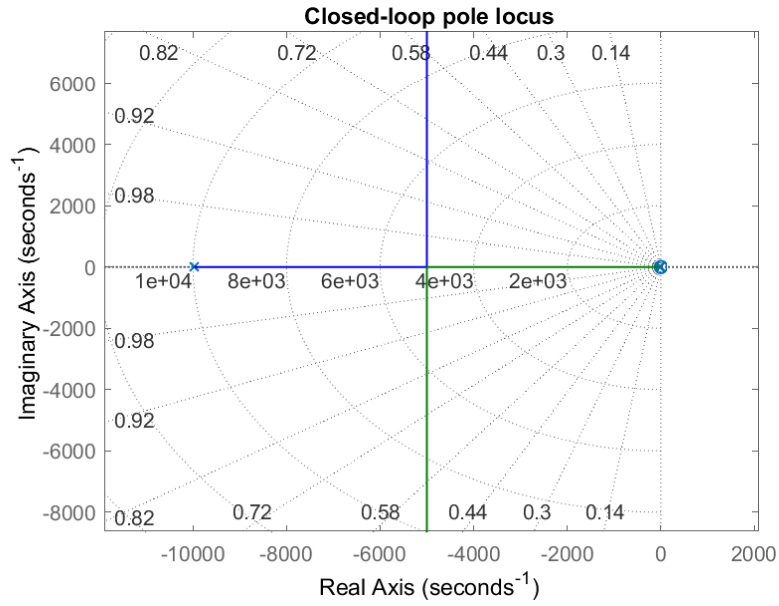


Figure 3.9: Locus of poles and zeros in closed loop of $G_{k_{p_v}}(s)$ as $k_{p_c} = 1/4$, $2k_{p_c}=k_{p_v}$ and $k_{i_v} = 1/2k_{p_c}$.

in the left half-plane. However, if any parameter from Table 3.1 is modified, the system response must be reanalyzed.

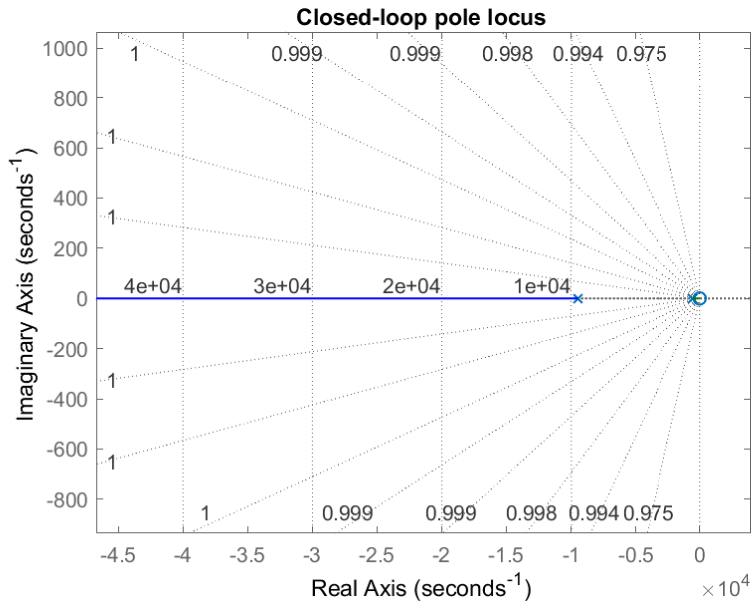


Figure 3.10: Locus of poles and zeros in closed loop of $G_{k_{i_v}}(s)$ as $k_{p_c} = 1/4$, $2k_{p_c}=k_{p_v}$ and $k_{i_v} = 1/2k_{p_c}$.

Chapter 4

Five-Level Asymmetrical T-Type Inverter and Active DC-link Voltage Balancing

Some multilevel inverters use DC-links formed by the series connection of capacitors. This helps to avoid large size, weight and inefficient transformers and rectifiers, or multiple DC voltage supplies, making them more efficient and of reduced components [21]. Nevertheless, voltage unbalance across the DC-link capacitors may occur due to multiple factors, including the inverter switching strategy, unbalanced AC loads, intrinsic characteristics of the topology itself or significant differences in the characteristics of the capacitors used, for example, variations in capacitance or equivalent series resistance. The typical topologies of multilevel inverters that use series connected capacitors DC-links are the Neutral Point Clamped Inverter (NPC), Flying Capacitor Inverter (FC) [21], and T-type Inverter [57]. In this chapter are discussed the Five-Level Asymmetrical T-Type (5L-ATT) inverter and their modulation scheme [58]. It is used to verify the capability of the studied converter to balance the DC-link capacitor voltages. Additionally, the simulation results are presented.

4.1 Asymmetrical T-type Inverter Description and Modulation Scheme

The 5L-ATT inverter [58] shown in Fig. 4.1, is based on the H-bridge inverter formed by the power switches S_1 , S_2 , S_3 and S_4 . It incorporates a bidirectional switch that consists in two power switches, S_5 and S_6 , and two diodes, D_1 and D_2 . The bidirectional switch is connected between the middle point of an H-bridge leg and the middle point of a two-capacitor series-connected DC-link formed by C_1 and C_2 . The 5L-ATT inverter can produce an output voltage of five levels.

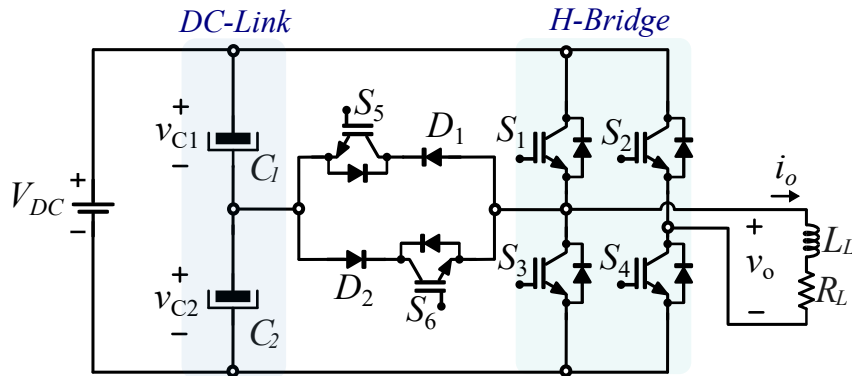


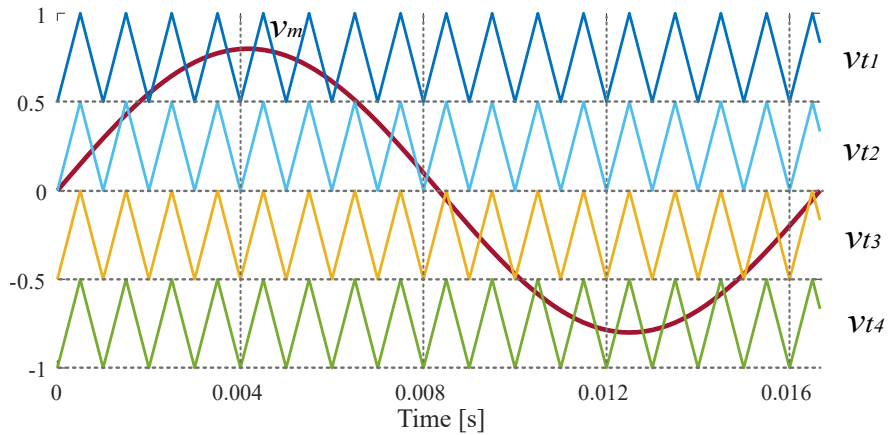
Figure 4.1: Schematic diagrams of the 5L-ATT inverter.

The five levels at the output voltage of the 5L-ATT inverter are generated by selectively connecting and disconnecting the capacitors in the DC-link through the different switching states. A balanced voltage across the C_1 and C_2 is essential. If this balance is lost, the quality of the output voltage waveform is affected. Considering that S_2 and S_4 are complementary, and the activation of S_5 and S_6 is equal, the total possible switching states are 2^4 . However, only six of those switching states are viable and are listed in Table 4.1.

Table 4.1: Switching states of 5L-ATT inverter.

State	Output voltage	Conducting devices
1	$+V_{DC}$	S_1, S_4
2	$v_{C2} = +V_{DC}/2$	S_4, S_6, D_2
3	0 V	S_3, S_4
4	0 V	S_1, S_2
5	$v_{C1} = -V_{DC}/2$	S_2, S_5, D_1
6	$-V_{DC}$	S_2, S_3

Considering the switching states shown in Table 4.1, and assuming that the power switches S_2 and S_4 operate in complementary mode, while S_5 and S_6 switch simultaneously, a modulation scheme based on Level-Shifted PWM with Phase Disposition (LS-PD-PWM) is defined. This method requires four level-shifted triangular carrier signals, denoted as $v_{t_i}(t)$, each with a peak amplitude of 0.5. A sinusoidal reference signal, $v_m(t)$, with a peak amplitude of 0.8 and centered at zero, is used for comparison. Figure 4.2 shows the corresponding waveforms and details of the modulation. The triangular signals, v_{t1} , v_{t2} , v_{t3} , v_{t4} , and v_{t5} , are compared to the sinusoidal reference, v_m , to generate the switching signals, v_{b1} , v_{b2} , v_{b3} , v_{b4} , respectively.

**Figure 4.2:** Triangular carrier signals v_{t_i} , $i = 1, 2, 3, 4$ and sinusoidal reference signal v_m .

Additionally, a signal v_{b5} is derived from the comparison of the sinusoidal reference with

a constant signal of zero amplitude. Finally, the final gate signals for the power switches are obtained using the boolean expressions defined in equations (4.1) to (4.3).

$$G_{S_1} = v_{b_1} \vee (v_{b_3} \wedge \neg v_{b_5}), \quad G_{S_3} = \neg v_{b_4} \vee (v_{b_5} \wedge \neg v_{b_2}) \quad (4.1)$$

$$G_{S_2} = \neg v_{b_5}, \quad G_{S_4} = \neg G_{S_2} \quad (4.2)$$

$$G_{S_5} = G_{S_6} = (\neg v_{b_1} \wedge v_{b_2}) \vee (\neg v_{b_3} \wedge v_{b_4}) \quad (4.3)$$

Figure 4.3 shows the switching sequence utilized for controlling the 5L-ATT inverter during two periods of the output voltage waveform. It can be observed that switches S_1 , S_3 , S_5 , and S_6 operate at high frequency, which is defined by the frequency of the triangular carrier signals. In contrast, switches S_2 and S_4 operate at the output voltage fundamental frequency.

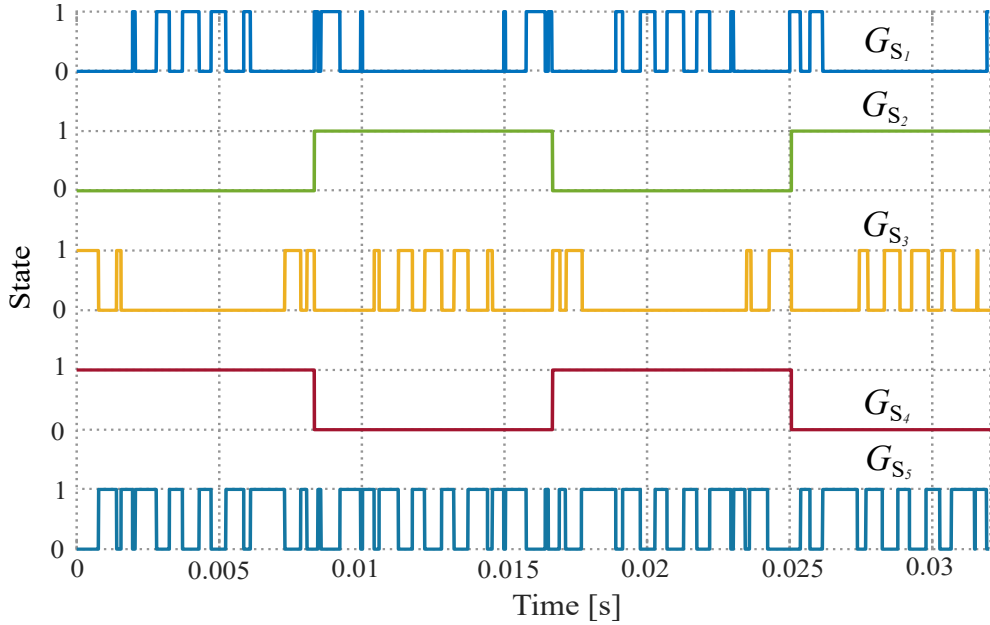


Figure 4.3: Switching sequence of the modulation scheme. In descending order, switching signals G_{S_1} , G_{S_2} , G_{S_3} , G_{S_4} , and $G_{S_5} = G_{S_6}$.

The switching sequence generated by equations (4.1) to (4.3) do not consider dead times. However, due to the turn on and turn off times of the power switches, simultaneous and complementary switching of the pairs S_1, S_3 , of S_2, S_4 , of S_1, S_5 , and of S_3, S_6 dead times must be included in those switching signal pairs to avoid short circuits across the DC voltage source or DC-link capacitors. This results in the definition of independent switching signals for S_5 and S_6 . The inclusion of dead times is proposed under the following considerations.

First, consider the positive semicycle of the output voltage waveform, v_o , which take values of V_{DC} , $V_{DC}/2$, and 0 V, corresponding to switching states one, two, and three in Table 4.1. Then a dead time is introduced between S_1 and S_5 , while keeping S_6 on during the dead time. Then, consider the negative semicycle of the output voltage waveform, v_o ,

which take values of 0 V, $-V_{DC}/2$, and $-V_{DC}$ corresponding to switching states four, five and six, in Table 4.1. Then a dead time is introduced between S_3 and S_6 , while keeping S_5 on during the dead time. Additionally, during the transitions between the positive and negative semicycles of the output voltage waveform, a dead time is introduced between the switching signals S_2 and S_4 . During this dead time, if the load current is positive then S_1 is turned on, if the load current is negative then S_3 is turned on.

Failure to properly activate the corresponding switch during the dead time may lead to abnormal variations in the output voltage, as undesired null switching states can be generated. These conditions may result in voltage distortions, increased stress on the power devices, and short circuits between DC-link capacitors segments. The boolean equations (4.4) to (4.9) are implemented to generate the previously described dead times incorporation.

$$G_{S_{1F}} = (G_{S_{1D}} \wedge \neg G_{S_1}) \wedge \neg(\neg(G_{S_{2F}} \vee G_{S_{4F}}) \wedge G_{S_4}) \vee G_{S_{3F}} \wedge \neg(\neg(G_{S_{2F}} \vee G_{S_{4F}}) \wedge G_{S_2}) \vee (G_{S_{1D}} \wedge \neg G_{S_1}), \quad (4.4)$$

$$G_{S_{2F}} = (\neg G_{S_4} \vee \neg G_{S_{4D}}) \wedge G_{S_{2D}}, \quad (4.5)$$

$$G_{S_{3F}} = (G_{S_{3D}} \wedge \neg G_{S_3}) \wedge \neg(\neg(G_{S_{2F}} \vee G_{S_{4F}}) \wedge G_{S_4}) \vee G_{S_{3F}} \wedge \neg(\neg(G_{S_{2F}} \vee G_{S_{4F}}) \wedge G_{S_2}) \vee (G_{S_{1D}} \wedge \neg G_{S_1}) \quad (4.6)$$

$$G_{S_{4F}} = G_{S_4} \wedge \neg G_{S_{4D}} \quad (4.7)$$

$$G_{S_{5F}} = (\neg(G_{S_{1D}} \wedge \neg G_{S_1}) \vee (G_{S_{5D}} \wedge \neg G_{S_5})) \wedge \neg G_{S_3} \wedge \neg G_{S_4} \vee (G_{S_{6D}} \wedge \neg G_{S_6}) \quad (4.8)$$

$$G_{S_{6F}} = (\neg((G_{S_{3D}} \wedge \neg G_{S_3}) \vee (G_{S_{6D}} \wedge \neg G_{S_6})) \wedge \neg G_{S_1}) \wedge \neg S_2 \vee (S_{5D} \wedge \neg G_{S_5}), \quad (4.9)$$

where $G_{S_{1F}}$ to $G_{S_{6F}}$ are switching signals that incorporate the dead times for each power switch. The signals $G_{S_{iD}}, i = 1, \dots, 6$, are obtained by delaying $G_{S_{iD}}$ an amount equal to the dead time.

4.2 Numerical Validations

The numerical validation of the converter operation, aimed at balancing the DC-link voltages of the 5L-ATT inverter, is presented. The system is tested under various operating conditions. First, the open-loop operation of the 5L-ATT inverter is tested with equal DC-link capacitors, and then under an abnormal condition emulated by connecting a resistor, R_r , in parallel with one of the DC-link capacitors. Subsequently, the same operating conditions are used with the converter connected between the DC voltage source and the DC-link capacitors; in this case, the converter operates in open-loop mode. Finally, the system is tested under the same conditions, but with the converter

operating in closed-loop mode. Figure 4.4 shows the diagram of the 5L-ATT inverter with the integrated converter. The parameters used for the numerical validation are listed in Table 4.2.

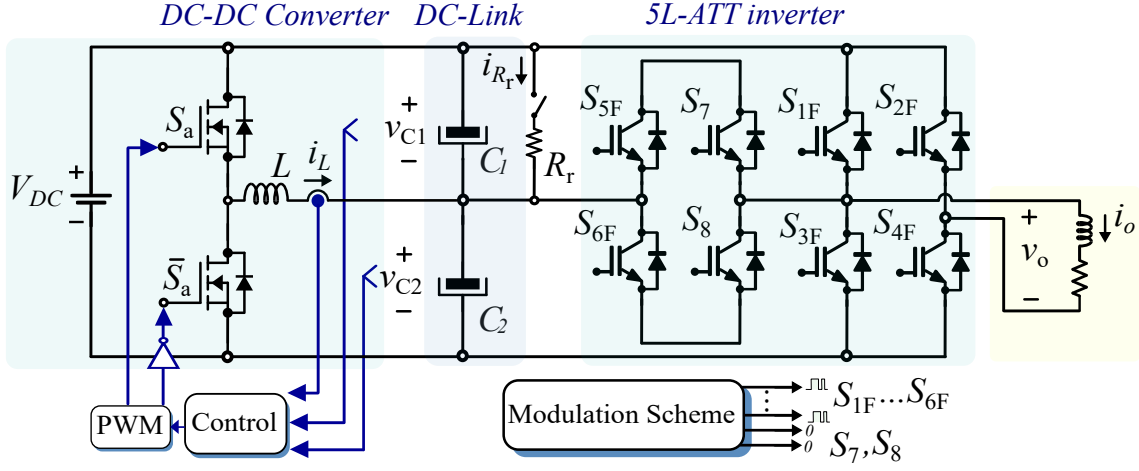


Figure 4.4: Schematic diagram of converter with 5L-ATTTL inverter.

Table 4.2: Numerical validations parameters of the converter and 5L-ATT inverter.

Element	Value
Input DC voltage source, V_{DC}	80 V
Inductor, L	2 mH
DC-link capacitor, C	1000 μ F
Resistor, R_r	20 Ω
Load resistor R_L	50 Ω
Inductor Load L_L	4 mH
5L-ATT inverter switching frequency f_{5L}	10 kHz
converter switching frequency f_s	20 kHz

4.2.1 Five-Level Asymmetrical T-Type Inverter

Figure 4.5 shows the voltages across capacitors C_1 and C_2 through the blue and red waveforms, respectively. The output current and voltage of the 5L-ATT inverter are represented by the red and blue waveforms. The output voltage exhibits five levels: -80 V, -40 V, 0 V, $+40$ V, and $+80$ V. The output current, which flows through an R_L load, is nearly sinusoidal. These waveforms indicate that the implemented modulation strategy does not lead to abnormal excursions in the output voltage or distortion in the output current.

In Fig. 4.6a shows the inverter response when C_1 is forced to discharge faster than C_2 by connecting R_r at approximately 0.2 s. This action results in voltage unbalance across the capacitors, output current distortion, and asymmetrical output voltage levels. Additionally, the capacitor voltages exhibit a transient response of approximately 60 ms. When R_r is disconnected, the voltages across the capacitors converge to $V_{DC}/2 = 40$ V, and the previously observed issues in the output current and voltage are resolved. However, the transient response lasts up to approximately 0.4 s, as shown in the capacitor voltage waveforms in Fig. 4.6b.

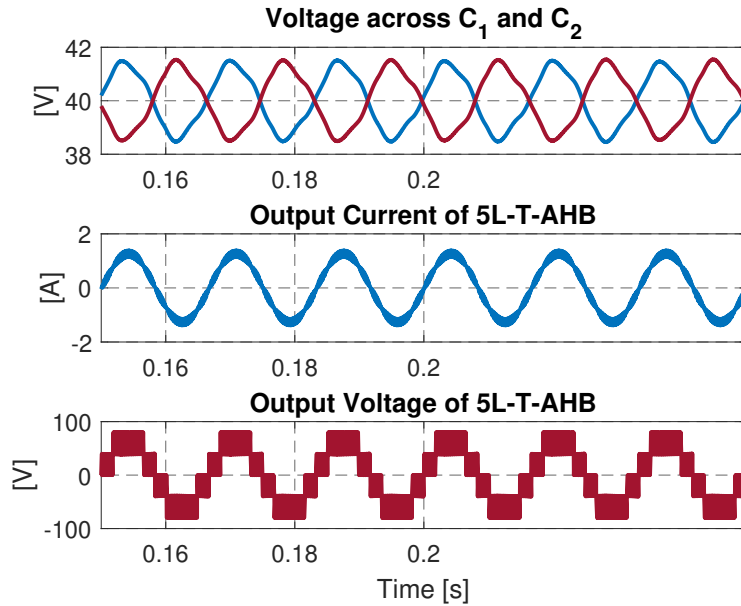


Figure 4.5: Steady states responses of 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the output current, and the output voltage.

4.2.2 Converter and Five-Level Asymmetrical T-Type Inverter both in Open-Loop Operation

Figure 4.7 shows the steady state responses of the voltages across capacitors C_1 and C_2 by the blue and red waveforms, respectively. Additionally, the current through the inductor, L , as well as the output current and voltage of the 5L-ATT inverter represented by the

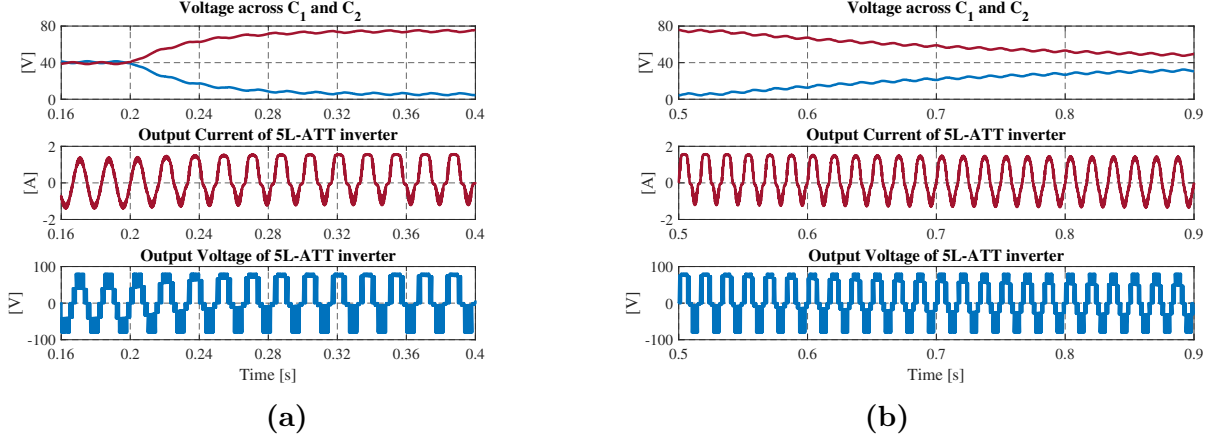


Figure 4.6: Transient states responses of 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the output current, and the output voltage. (a) When R_r is connected (b) When R_r is disconnected.

green, red, and blue waveforms, respectively. These results demonstrate proper voltage balancing of the DC-link in the 5L-ATT inverter. The current through L exhibits a grid frequency AC component, and its peak magnitude corresponds to the inverter output current, superimposed with a ripple due to the switching of the converter. Figure 4.8

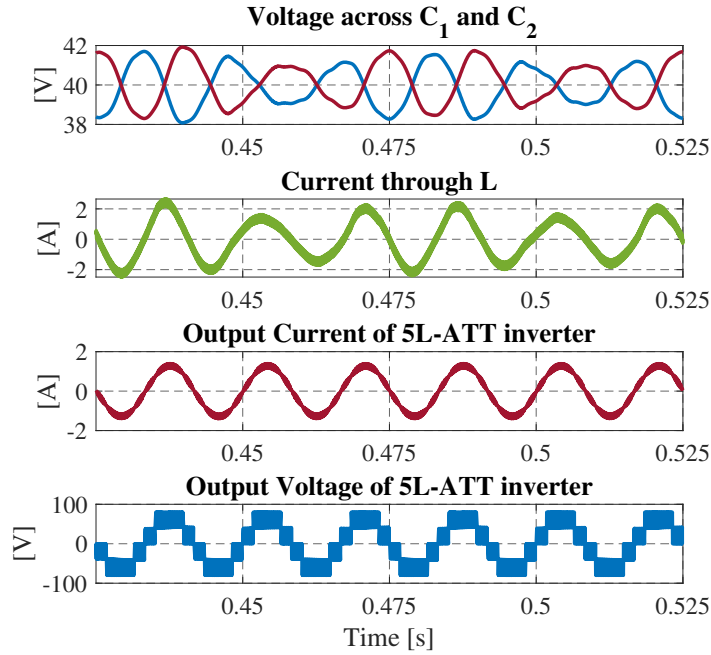


Figure 4.7: Steady states responses of the converter operating in open-loop mode and 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the current through the inductor, L , the output current, and the output voltage.

shows the transient state responses. Specifically, Fig. 4.8a shows the behavior of the system when the resistor R_r is connected, Fig. 4.8b presents the responses after the disconnection of R_r . The plotted waveforms correspond to the voltages across capacitors C_1

and C_2 , the current through L , the current through the resistor R_r , i_{R_r} , and the output current and voltage of the 5L-ATT inverter, represented by the blue, cyan, green, light blue, red, and blue curves, respectively. When the resistor R_r is connected, the transient response lasts approximately 10 ms, and the voltages across the capacitors have oscillations with a peak amplitude of 38 V and 42 V. Once R_r is disconnected, the voltages across C_1 and C_2 have the same behavior. Additionally, the connection of R_r introduces a negative DC offset in i_L , whose magnitude corresponds to the value of i_{R_r} .

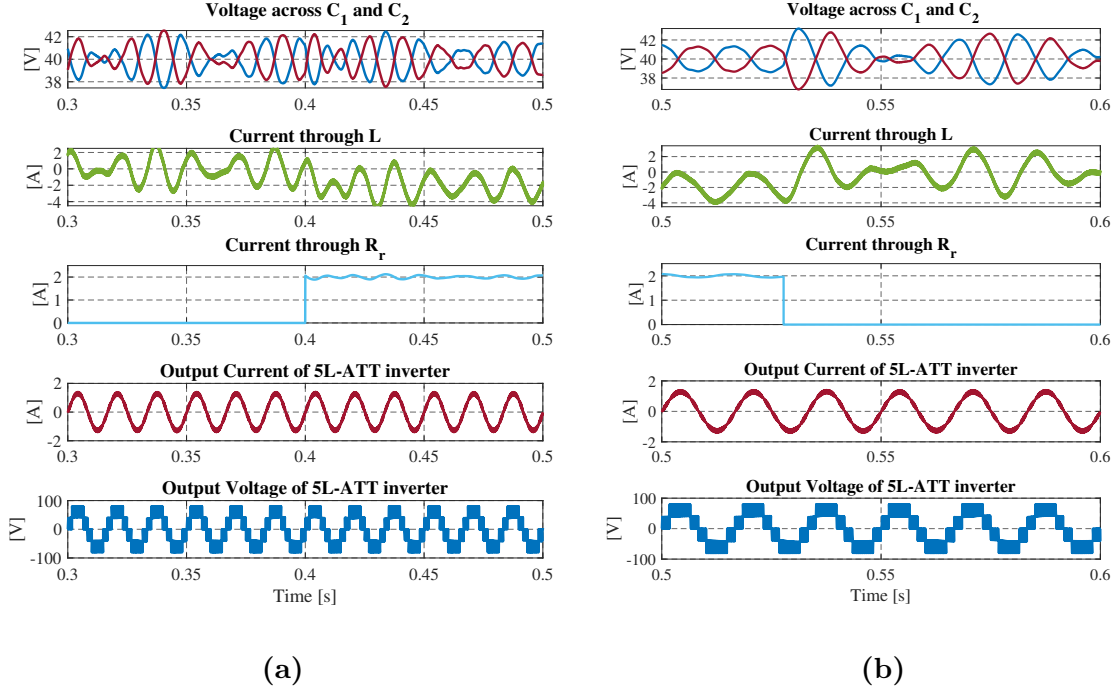


Figure 4.8: Transient states responses of the converter operating in open-loop mode and 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the current through the inductor, L , the current through R_r , the output current, and the output voltage. (a) When R_r is connected (b) When R_r is disconnected.

4.2.3 Converter in Closed-Loop Together with the Five-Level Asymmetrical T-Type Inverter in Open-Loop

Figure 4.9 shows the steady state responses of the voltages across capacitors C_1 and C_2 by the blue and red waveforms, respectively. Additionally, the current through the inductor, L , as well as the output current and voltage of the 5L-ATT inverter represented by the green, red, and blue waveforms, respectively. These results demonstrate the action of the voltage balancing of the DC-link in the 5L-ATT inverter. Additionally, the inductor current exhibits a grid-frequency AC component, and its peak magnitude corresponds to the inverter output current, superimposed with a ripple due to the switching of the converter.

Figure 4.10 shows the transient state responses. Specifically, Fig. 4.10a shows the behavior of the system when the resistor R_r is connected, Fig. 4.10b presents the responses after the disconnection of R_r . The resistor R_r is introduced into the circuit, the capacitor voltages exhibit a transient lasting approximately 15 ms, converging to $v_{C1} = v_{C2} = 40$ V. The output voltage levels of the inverter remain unaffected and maintain their symmetrical behavior. After disconnecting R_r , both capacitor voltages converge to the same voltage 40 V. Additionally, the connection of R_r causes a negative DC offset in the inductor current i_L , whose amplitude matches that of the current i_{R_r} .

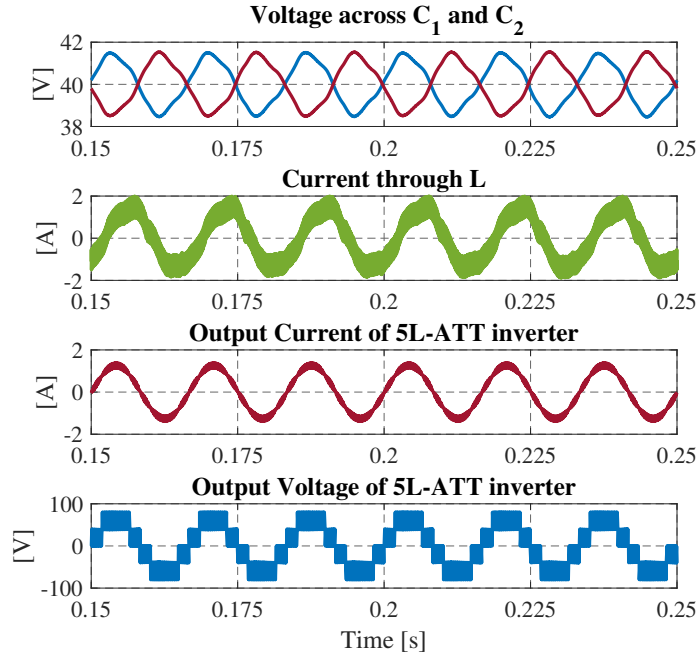
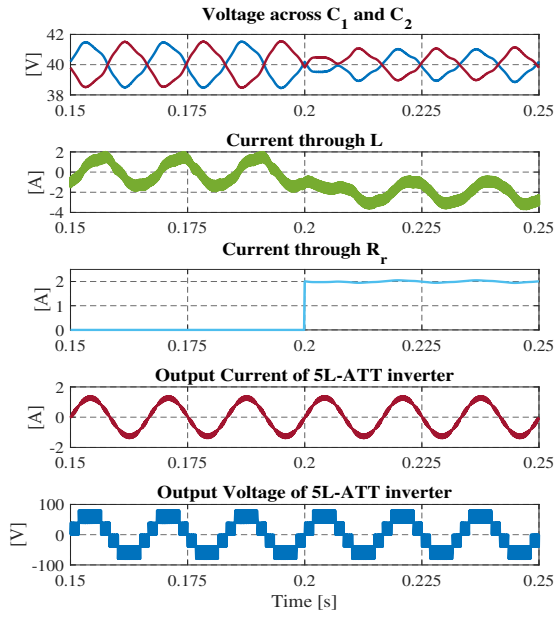
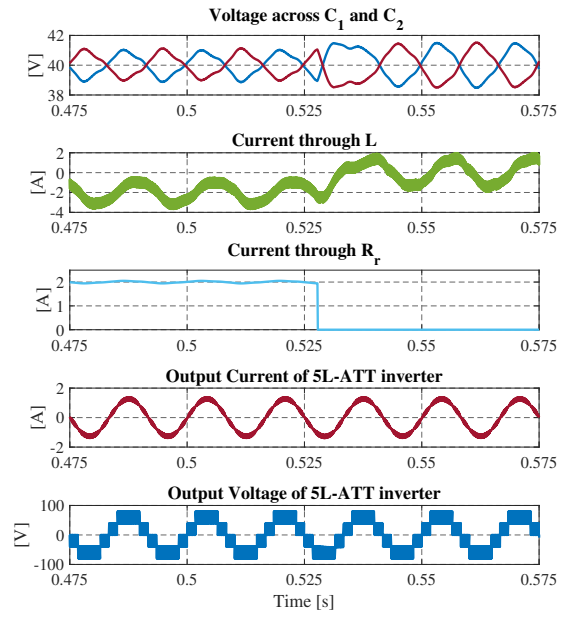


Figure 4.9: Steady states responses of the converter operating in closed-loop mode and 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the current through the inductor, L , the output current, and the output voltage.



(a)



(b)

Figure 4.10: Transient states responses of the converter operating in closed-loop mode and 5L-ATT inverter. In descending order, voltage across C_1 and C_2 , the current through the inductor, L , the current though R_r the output current, and the output voltage. (a) When R_r is connected (b) When R_r is disconnected.

Chapter 5

Laboratory Prototype and Experimental Results

In this chapter, the design and implementation of a laboratory prototype of a converter intended for DC-link voltage balancing in a 5L-ATT inverter system are presented. The complete setup is used to obtain experimental results that validates the proposal of this thesis. The 5L-ATT inverter is operated in open-loop as described in Chapter 4. Its modulation scheme is implemented using the Altera Cyclone IV EP4CE22F17C6N FPGA and the programming is carried out using Quartus II. The converter prototype includes circuits for sensing the DC-link capacitor voltages and the DC side inductor current. The proposed control scheme is implemented using the TMS320F28379D DSP circuit under Matlab/Simulink. Additionally, the program utilizes the Simulink *Monitor & Tune* option, which allows real-time adjustment of control gains. The communication of switching signals generated by the DSP circuit are done thru an interface board that optically isolates the DSP circuit and the converter.

5.1 Laboratory Prototype Implementation

Figure 5.1 shows the laboratory prototype. It consists of voltage and current sensing circuits, an interface board, the converter, and the 5L-ATT inverter. In the following section of this chapter, the design and implementation of each board are presented. The implementation of the converter includes the proposed control scheme. In the case of the 5L-ATT inverter, the modulation scheme is presented.

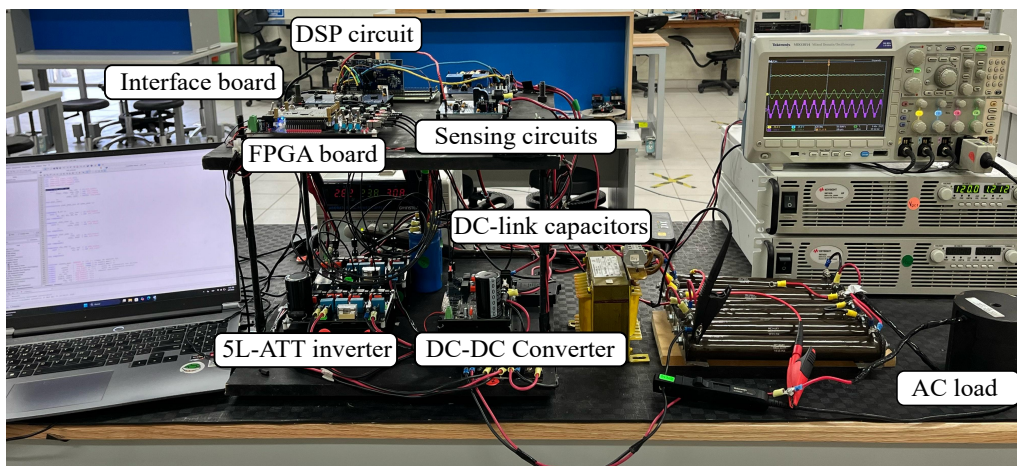


Figure 5.1: Laboratory prototype.

5.1.1 Voltage and Current Sensing Circuit

This section presents the design and implementation of converter sensing circuits based on operational amplifiers. The key physical variables that are required for closed-loop operation are the inductor current, and the two voltages across the DC link capacitors. Since the TMS320F28379D DSP is utilized, the sensing circuits adjust the voltage and current signals to match the DSP ADC ports operational range of 0 V to 3.3 V.

Current sensing circuit is built using the LTS 15-NP current transducer and operational

amplifiers (Op-Amp) TL082 and OPA295. Figure 5.2 presents the electrical diagram design. The LTS 15-NP is a Hall effect current transducer, offering galvanic isolation and the capability to measure AC, DC, and pulsed currents with a peak magnitude of 15 A. The LTS 15-NP requires a 5 V power supply. According to the manufacturer datasheet [59], the output voltage of LTS 15-NP is fixed by,

$$V_{O_{LTS}} = 2.5 \text{ V} \pm (0.625 \cdot I_P / I_{PN}), \quad (5.1)$$

where I_P is the measured current and I_{PN} is the primary nominal current.

The transducer output voltage $V_{O_{LTS}}$ is processed by an Op-Amp circuit formed by several stages. Firstly, an inverting amplifier configuration followed by a first-order low-pass filter of unitary DC gain, and a voltage follower configuration. This results in a signal in the 0 V to 3.3 V range. Those circuit stages are denoted by the names U_1 , U_2 and U_3 , respectively, in Fig. 5.2. This circuit stages are described with more detail in what follows.

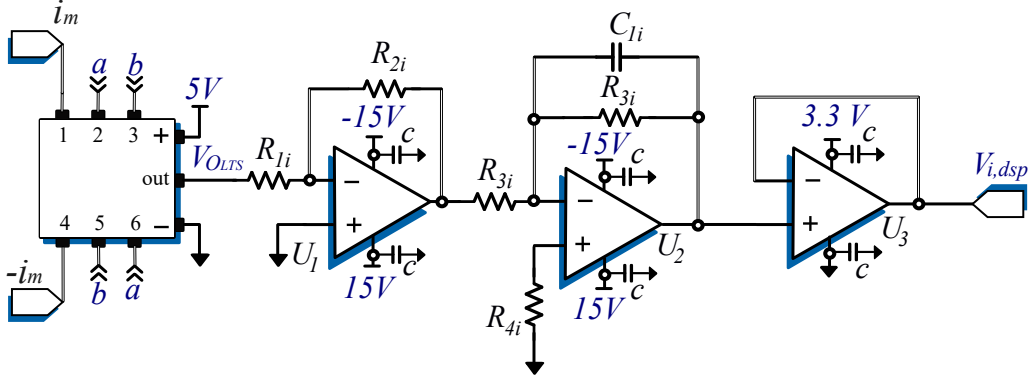


Figure 5.2: Diagram of current sensing circuit.

The output voltage $V_{O_{LTS}}$ of the LTS 15-NP transducer is in the range of 0 V to 5 V and the U_1 gain is 0.606. This is used to convert this output to the range of 0 V to 3.3 V. The circuit U_2 is an anti-aliasing filter which limits the bandwidth of the sensed signals, and avoids high frequency noise into the DSP ADC ports. The output voltage of U_3 follows the voltage of the output of U_2 but has a supply of 3.3 V which limits the rail-to-rail output to this range. The output voltage of the circuit, $V_{i,dsp}$, can be described by,

$$f(v_{i,dsp}) = \begin{cases} 3.3 \text{ V} & \text{if } v_{i,dsp} > 3.3 \text{ V}, \\ v_{i,dsp} & \text{if } 0 \leq v_{i,dsp} \leq 3.3 \text{ V}, \\ 0 & \text{if } v_{i,dsp} < 0, \end{cases} \quad (5.2)$$

where $v_{i,dsp} = V_{O_{LTS}} \cdot 0.606$. The voltage supply to the complete sensing circuit is 24 V from which lower voltage levels are obtained for the distinct circuits using isolated converter modules with regulated outputs. The TracoPower TMR2423 is used to supply the TL082 Op-Amps, while the TracoPower is used TSR-1-2433 for the OPA295 Op-Amps

and TracoPower TMA2405S to supply the LTS 15-NP transducer. The resistor and capacitor values of the circuit in Fig. 5.2 are set as follows, $R_{1i} = 50 \text{ k}\Omega$, $R_{2i} = 3 \text{ k}\Omega$, $R_{3i} = 100 \text{ }\Omega$, $R_{4i} = 50 \text{ }\Omega$, $C = 100 \text{ nF}$ and $C_{1i} = 0.15 \text{ }\mu\text{F}$.

The voltage transducer LV-25 and Op-Amps TL082 and OPA295 are used in the voltage circuit. Figure. 5.3 shows the schematic diagram of the design. The LV-25 transducer provides galvanic isolation between the power electronic circuit and the control. The LV-25 transducer requires a bipolar supply voltage of 12 V. To measure voltage, a current, I_{PN} , proportional to the measured voltage, must be applied through an external resistor, R . Additional features of the LV-25 include the ability to measure DC and AC voltage with maximum magnitude of 500 V, a nominal primary current of $I_{PN}=10 \text{ mA}$, and a current ratio of 2.5 between the I_{PN} and output current, I_{OLV25} .

Given that $I_{OLV25} = 25 \text{ mA}$, the resistor R_{1v} is selected to set the output voltage $V_{v,dsp}$ within the range of 0 to 3.3 V. Additionally, the circuit U_1 implements an anti-aliasing filter that limits the bandwidth of the sensed signal preventing high-frequency noise from entering the DSP ADC inputs. The circuit U_2 is a voltage follower supplied by 3.3 V, ensuring that the rail-to-rail output remains within this voltage range. The output voltage of the entire circuit, $V_{v,dsp}$, can be expressed as:

$$f(v_{v,dsp}) = \begin{cases} 3.3 \text{ V} & \text{if } v_{v,dsp} > 3.3 \text{ V}, \\ v_{v,dsp} & \text{if } 0 \leq v_{v,dsp} \leq 3.3 \text{ V}, \\ 0 & \text{if } v_{v,dsp} < 0, \end{cases} \quad (5.3)$$

where, $v_{v,dsp} = R_{1v} \cdot I_{OLV25} \cdot 2.5$, I_{OLV25} is equal to the measured voltage, v_m to $-v_m$, multiplied by R_v . Complete sensing circuit voltage supply is 24 V from which lower voltage levels are obtained for the distinct circuits using isolated converter modules with regulated outputs. The TracoPower TMR2423 is used to supply the TL082 Op-Amps and transducer LV-25, and the TracoPower TSR-1-2433 for the OPA295 Op-Amps. The resistor and capacitor values of the circuit, in Fig. 5.2, are set as follows, $R_v = 49 \text{ k}\Omega$, $R_{1v} = 133 \text{ }\Omega$, $R_{2v} = 470 \text{ }\Omega$, $C = 100 \text{ nF}$ and $C_{1v} = 4.7 \text{ nF}$.

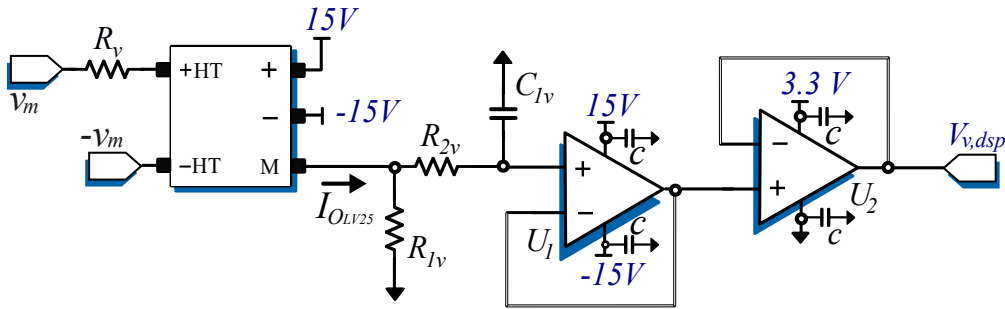


Figure 5.3: Diagram of voltage sensing circuit.

5.1.2 Interface board

The management of the switching signals that are generated by the TMS320F28379D DSP, is carried out using a board whose schematic diagram shown in Fig. 5.4. It requires a 5 V DC power supply and is built from a 74LS541 buffer, SN75452B opto-drivers and HFBR-1531Z transmitters.

The 74LS541 buffer features a 5 V power supply and three-state outputs: high impedance, high, and low voltage levels. The buffer circuit prevents excessive current demand to the TMS320F28379D DSP. The high impedance output state is fixed by the output of an two input internal AND logic gate. These inputs are set to a low voltage level, to obtain the switching singals generated by the DSP at the ouputs of the buffer.

The SN75452B opto-driver and HFBR-1531Z transmitter guarantee optical isolation between the DSP circuit and the converter. Additionally, the transmission of the switching signals through fiber-optic cables minimizes losses and avoids interference or parasitic components commonly found in traditional wired connections. Each HFBR-1531Z transmitter is controlled by an SN75452B opto-driver.

The SN75452B opto-driver is able to handle up to 300 mA at its outputs and has a high-speed switching capability. The resistor values in Fig. 5.4 are set as follows $R_1 = 1 \text{ k}\Omega$ and $R_2 = 10 \text{ k}\Omega$.

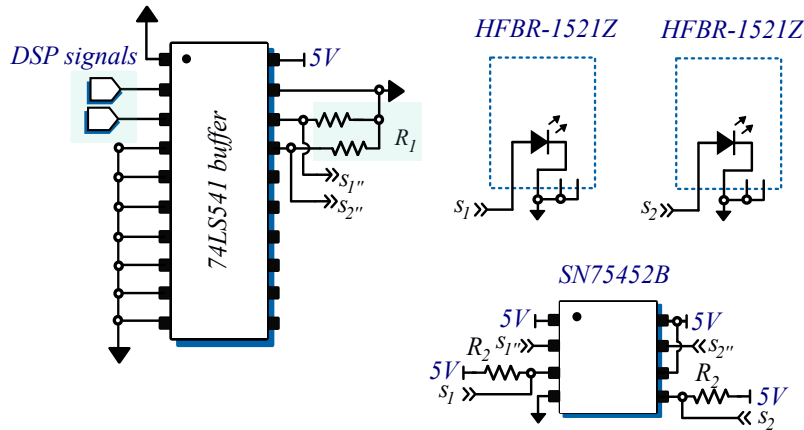


Figure 5.4: Schematic diagram of interface board.

5.1.3 DC-DC Converter

The design and implementation of the converter laboratory prototype consider the use of two IRFP406A MOSFETs. The control signal for each MOSFET is transmitted using an HFBR-2531 optical fiber receiver and an HCPL-3120 opto-driver, as shown in Fig. 5.5.

The main electrical features of the IRFP460A MOSFET include a drain-to-source voltage of 500 V, a drain current of 20 A, a drain-to-source on resistance of $0.27 \text{ }\Omega$, and a high-speed switching capability, with a turn-on delay time of 18 ns and a turn-off delay time

of 45 ns. The IRFP406A is typically used in switch mode power supply applications such as full-bridge inverters and Power Factor Correction (PFC) boost converters.

The HFBR-2531 requires 12 mA and 5 V as source supply and it is open collector. Resistor $R_f = 390 \Omega$ is used to fix the voltage at its collector. The power supply of the HCPL-3120 has been fixed as a dual voltage, provided by the Murata MGJ2D051505SC, with voltages of +15 V and -5 V. The value of R_1 is fixed to 330Ω that assures the current required by the HCPL-3120 for its optimal operation. Additionally, a LED is connected between the fiber optic receiver and the opto-driver to indicate the reception of switching signals through the fiber optic.

The gate resistor R_G is essential for controlling the switching speed of the MOSFETs by regulating the charging and discharging of its parasitic capacitance. Proper selection of R_G enhances performance, limits gate driver current, reduces gate ringing, and prevents unwanted turn-on events, ensuring efficient and reliable operation.

Therefore, the gate resistance R_G is implemented as two separate resistors R_{on} and R_{off} , with the addition of a fast recovery diode 1N4148, denoted as D_{off} . This configuration is used based on the guidelines presented in [60]. The selection of these resistors takes into account the peak current limitations of the HCPL-3120 gate driver and the corresponding supply voltage levels. The resistor values are determined using equation (5.4),

$$R_{off} = \frac{+15 \text{ V} - (-5 \text{ V})}{I_{Gdp}}, \quad I_{Gdp} < I_{OLpeak}, \quad (5.4)$$

where I_{OLpeak} is the maximum allowable low-side peak output current of the HCPL-3120, which is equal to 2 A. The gate discharge current I_{Gdp} flows through R_{off} during the MOSFET turn-off transition. The value of R_{on} is selected as twice the value of R_{off} , i.e., $R_{on} = 2 \cdot R_{off}$. The resistor values used in the implementation are: $R_{on} = 33 \Omega$, $R_{off} = 16 \Omega$, and an additional resistor $R_2 = 220 \Omega$.

5.1.4 Controller Implementation Platform

Matlab/Simulink software and a Texas Instruments TMS320F28379D DSP are used to implement the proposed control scheme, whose schematics are shown in Fig. 5.6. The implementation uses the *Monitor & Tune* option, which allows real-time adjustment of controller gains and some constant blocks. The control scheme is realized in Simulink using ADC blocks, *Two Degrees-Of-Freedom* (2DOF) PID controller and the *Enhanced Pulse Width Modulator* (ePWM) block.

The implementation allows to test the converter in open-loop as well as in closed-loop. It incorporates a protection block that is based on relational operators and OR gates, and it is activated when voltage or current overshoots are detected during closed-loop operation. If an overshoot is detected, the converter switches back to open-loop operation.

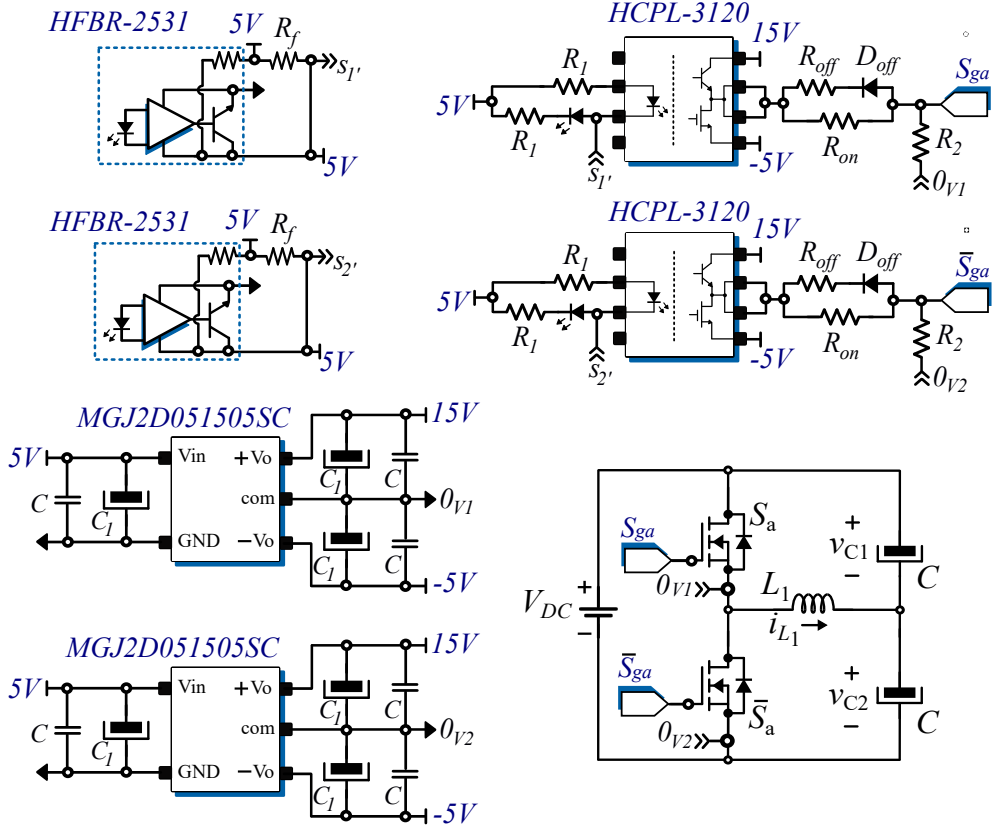


Figure 5.5: Schematic diagram of converter laboratory prototype.

The controller implementation is designed to initially operate the converter in open-loop mode, and then, the user can change its operation to closed loop by changing the value of an internal signal.

The ePWM block is used to generate the PWM signal required for converter operation. This block operates in up-down counting mode, which results in a symmetrical triangular carrier waveform. The output signal frequency is determined by (5.5),

$$T_p = \frac{100 \text{ MHz}}{2 \cdot f_s \cdot TBPRD \cdot HSPCLKDIV}, \quad (5.5)$$

where T_p denotes the timer period, f_s is the converter switching frequency, $TBPRD$ represents the time-base period register, and $HSPCLKDIV$ corresponds to the high-speed time-base clock prescaler divider. In this implementation, the switching frequency is fixed at 20 kHz and the ePWM1A and ePWM1B ports are enabled with deadband.

The ADC ports of the TMS320F28379D DSP are enabled to acquire the sensed DC voltages and current. In this case, module A is activated using the ADCIN0, ADCIN1, and ADCIN3 input channels. ADCIN0 and ADCIN1 are used to acquire the voltages across the capacitors, while ADCIN3 is used to acquire the current through the inductor. Module A is configured with 12-bit resolution and a sampling time of 1/300 kHz. The voltage and current values acquired by the ADC ports are represented as digital values

in the range of 0 to 4095 bits. Equations (5.6), (5.7), and (5.8) are used to convert these digital values into the voltages across C_1 , C_2 , and the inductor current, respectively.

$$G_{ADCIN0} = \left(\frac{3.3}{4096} \cdot \frac{1500}{3} \right) - \frac{45}{26} \quad (5.6)$$

$$G_{ADCIN1} = \left(\frac{3.3}{4096} \cdot 120 \right) + 0.6 \quad (5.7)$$

$$G_{ADCIN2} = \left(\frac{3.3}{4096} - 1.65 \right) \left(\frac{-1}{0.0825} \right) \quad (5.8)$$

The proposed control scheme uses a PI controller for voltage regulation and a P controller for current control. A PID controller (2DOF) block is used to implement the PI voltage control, while a gain block is used for the proportional current control. The PI controller is configured in discrete time and includes external inputs to allow real-time gain adjustments through constant variable blocks. Additionally, an external reset is implemented for the integral action, which is triggered on a falling edge.

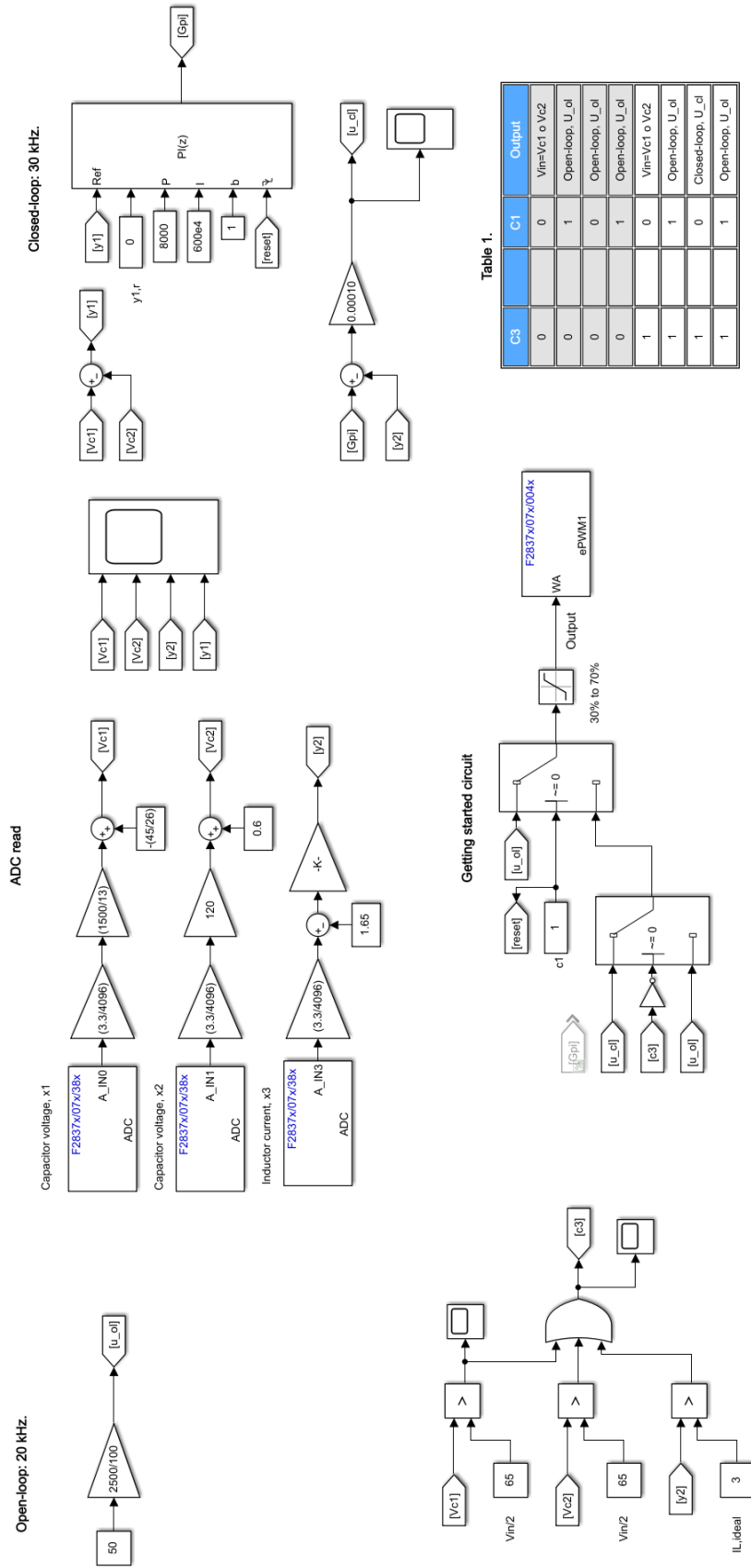


Figure 5.6: Control scheme implemented in Matlab/Simulink.

5.1.5 Asymmetrical T-type Inverter and its Modulation Scheme

The laboratory prototype of the 5L-ATT inverter is built using two H-Bridge inverters. Figure 5.7 shows their connection. The bidirectional switch is implemented using the $H\text{-Bridge}_1$, where S_7 and S_8 are not switched, that is their gate signals are set to zero volts, but S_7 and S_8 antiparallel diode can be in conduction. On the other hand, the $H\text{-Bridge}_2$ forms the H-Bridge inverter of 5L-ATT. The design details of each H-Bridge prototype are described in [61].

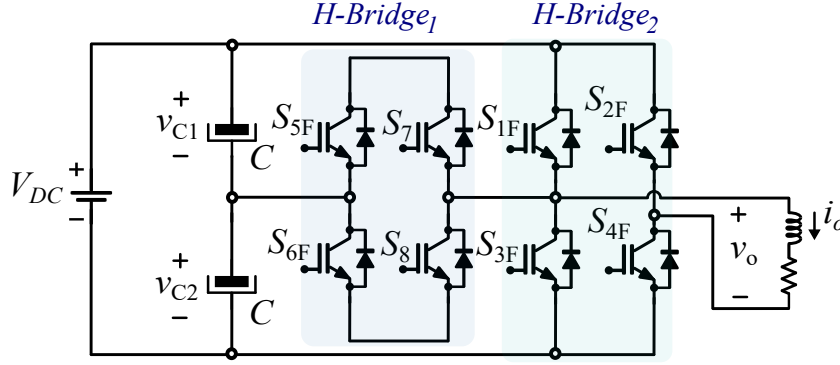


Figure 5.7: Schematic diagram of 5L-ATT inverter.

The proposed modulation scheme for the 5L-ATT inverter is implemented using the Altera Cyclone IV EP4CE22F17C6N FPGA, in the DE0-Nano development board. Additionally, Table 5.1 shows a summary of the FPGA compilation results. The design process was carried out in VHDL using Quartus II and Matlab. Figure 5.8 presents the block diagram of the modulation scheme. This modulation scheme adopts a five-stage pipelined architecture, fully synchronized by an internal clock signal, clk , and a reset input, rst [62]. The clk signal is connected to the internal clock of the FPGA, and external reset signal is used to initiate or clear the programming process.

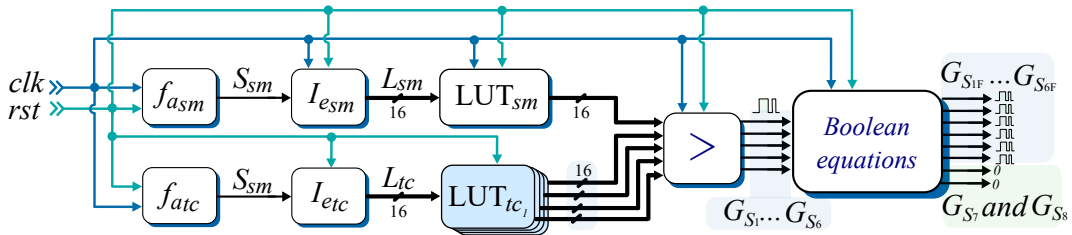


Figure 5.8: Block diagram of modulation scheme of 5L-ATT inverter.

The five-stages include: two frequency accumulator blocks denoted as f_{asm} and f_{atc} , two input enable blocks, I_{esm} and I_{etc} , five Look-Up Tables (LUTs), LUT_{sm} , and LUT_{tc_i} , $i = 1, \dots, 4$. The contents of the LUT were computed in MATLAB and subsequently implemented in Quartus II using VHDL. Additionally, one comparison block, and one block where boolean equations are implemented to generate the dead times required in the inverter operation. The blocks f_{asm} , I_{esm} and LUT_{sm} are used to generate a sinusoidal

reference signal. While the blocks f_{atc} , I_{etc} together with each of the blocks LUT_{tc_i} , $i = 1, \dots, 4$ are used to generate four triangular carrier signals.

Table 5.1: Quartus II compilation results.

Parameter	Value
Timing models	Final
Total logic elements	444 / 22,320 (2%)
Total combinational functions	443 / 22,320 (2%)
Dedicated logic registers	96 / 22,320 (<1%)
Total registers	96
Total pins	10 / 154 (6%)
Total virtual pins	0
Total memory bits	0 / 608,256 (0%)
Embedded multiplier 9-bit elements	0 / 132 (0%)
Total PLLs	0 / 4 (0%)

In the first stage, the frequency accumulator blocks f_{asm} and f_{atc} generate signals corresponding to the frequency of the sinusoidal reference, S_{sm} , and to the triangular carrier signals, S_{tc} , respectively. Their operation is based on an up-counter that increments with each rising edge of the FPGA clock. When the counter reaches its limit, F_{ref} , a pulse is produced to enable the subsequent blocks, I_{esm} and I_{etc} . The counter limit, F_{ref} , is defined by,

$$F_{ref} = \frac{F_{FPGA}}{2^M F_w} - 2, \quad (5.9)$$

where F_{FPGA} is the FPGA clock frequency equal to 50 MHz, M is the bit resolution of the respective accumulator equal to 16 bits and F_w is the desired output frequency. The f_{atc} block generates a pulse signal with a fixed frequency of 10 kHz, and a counter range of $[0, 12]$. On the other hand, f_{asm} generates a pulse signal with a fixed frequency of 60 Hz, and a counter range of $[0, 3254]$.

In the second stage, the input enable blocks, I_{esm} and I_{etc} , operate as 16 bits up-counters. Up on initialization, the counter increments from 0000H to FFFFH, with the current count value presented on the output buses L_{sm} and L_{tc} . These output values are used in the third stage, as the inputs for the LUT blocks, and they are used to address the positions in the LUTs to generate the amplitude values corresponding to the sinusoidal reference signal and the triangular carrier signal, (5.10) and (5.11), respectively. The binary coded value of the amplitude of those signals are obtained using Matlab by calculating the normalized sine and triangular functions with 256 points over the interval $[0, 2\pi)$. Each value is encoded using a 2QN format of 16 bits: two bits for the sign and integer part, and fourteen bits for the fractional part. In the LUTs, the amplitude, phase, and offset are specified using (5.10) and (5.11),

$$F_{mod}(i) = A_m \sin\left(\frac{2i(i-1)\pi}{D}\right), \quad (5.10)$$

$$F_{car}(i) = A_c \text{ sawtooth}\left(\frac{2i(i-1)\pi}{D} - X, \frac{1}{2}\right) + Y, \quad (5.11)$$

where F_{mod} is the sampled modulating signal, F_{car} is the sampled carrier signal, A is the signal amplitude, Y is the signal offset, i is the input index from the enable block, D is a 16 bit value representing the number of LUT samples, and X is the signal phase shift in bits. In this design the amplitude of A_m is set to 0.8 and that of A_c to 0.25.

In the fourth stage the comparison between the amplitudes of each carrier to the amplitude of the modulating signal, is performed, generating five different switching signals. In the last stage, the boolean equation block is utilized to generate the required dead times. The logical equations implemented within this block are described in Chapter 4.

5.2 Experimental results

The experimental results of the converter operation aimed at balancing the DC-link voltages of the 5L-ATT inverter are presented. Different operating conditions are tested. First, the open-loop operation of the 5L-ATT inverter is tested under equal DC-link capacitors and then under an abnormal condition that is emulated by connecting to a single DC-link capacitor a parallel resistor. Then, the same operation conditions are also tested in closed-loop operation. The results is obtained under the three following test cases: 5.2.1. Operation of the 5L-ATT inverter alone, 5.2.2. Operation of the 5L-ATT inverter along with the converter, both in open-loop mode, and 5.2.3. Operation of the 5L-ATT inverter in open-loop and the converter in closed-loop mode. The parameters used in the experiments are listed in Table 5.2.

Table 5.2: Experimental parameters of the converter and 5L-ATT inverter.

Element	Value
Input DC voltage source, V_{DC}	80 V
Inductor, L	2 mH
DC-link capacitor, C	1000 μ F
Load resistor R_L	50 Ω
Inductor Load L_L	4 mH
5L-ATT inverter switching frequency f_{5L}	10 kHz
Converter switching frequency f_s	20 kHz

5.2.1 Five-Level Asymmetrical T-Type Inverter

The diagram of the prototype configuration used to test the operation for the 5L-ATT inverter without the converter is shown in Fig. 5.9. The 5L-ATT inverter operates in open-loop mode with the switching signals generated by the EP4CE22F17C6N FPGA.

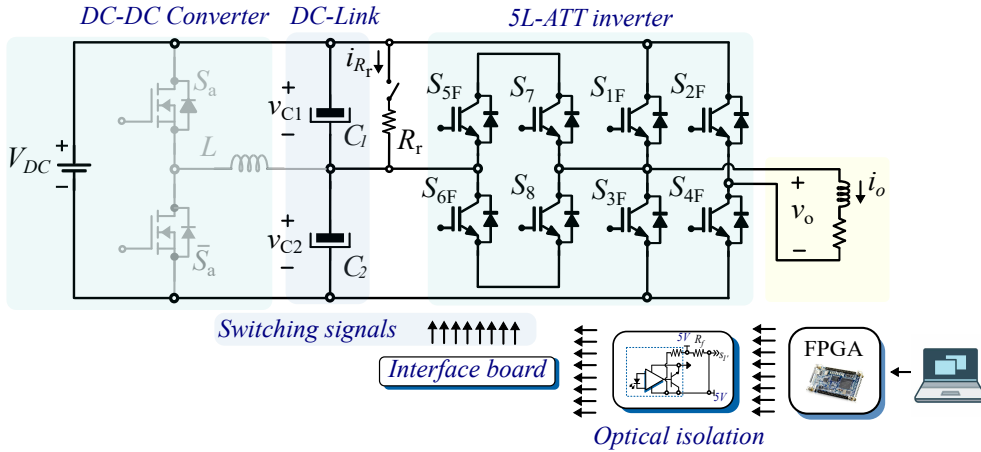


Figure 5.9: Diagram of the 5L-ATT inverter without the converter.

Figure 5.10a shows the switching pattern with a dead time of 20 ns and a switching frequency f_{5L} fixed at 10 kHz. Figure 5.10b presents the same switching pattern but with f_{5L} set to 1 kHz, allowing for better visualization of the switching events. In Fig. 5.10, eight switching signals are displayed, where the last two signals, labeled as S_7 and S_8 ,

remain at a logic level of 0.

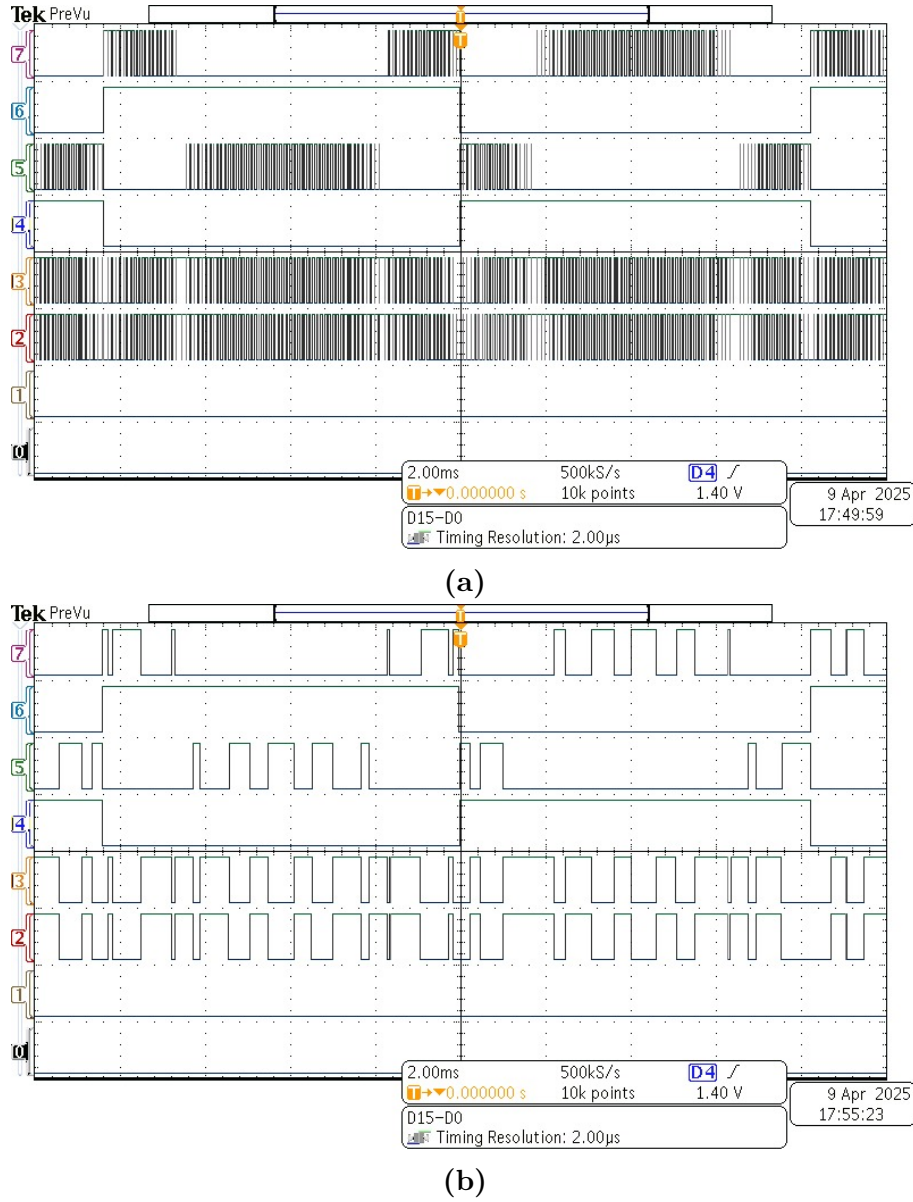


Figure 5.10: Switching pattern of the modulation scheme of 5L-ATT inverter (x-axis fixed at 2 ms/DIV). In descending order, switching signals of S_{1F} , S_{2F} , S_{3F} , S_{4F} , S_{5F} , S_{6F} , S_7 , and S_8 , respectively. (a) $f_{5L} = 1$ kHz and (b) $f_{5L} = 10$ kHz.

Figure 5.11 shows the voltages across capacitors C_1 and C_2 through the cyan and blue waveforms, respectively. The output current and voltage of the 5L-ATT inverter are represented by the green and pink waveforms. The output voltage exhibits five levels: -80 V, -40 V, 0 V, $+40$ V, and $+80$ V. The output current, which flows through an RL load, is nearly sinusoidal. These waveforms indicate that the implemented modulation strategy does not lead to abnormal excursions in the output voltage or distortion in the output current.

In Fig. 5.12a shows the inverter response when C_1 is forced to discharge faster than C_2 by

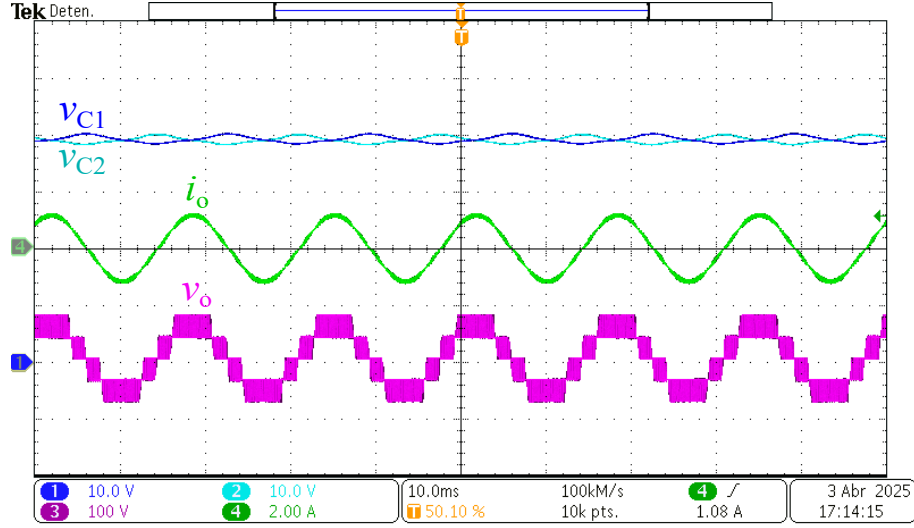


Figure 5.11: Steady states responses of 5L-ATT inverter. In descending order, voltage across C_1 and C_2 (y-axis 10 V/DIV, x-axis fixed at 10 ms/DIV). The output current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV). The output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV).

connecting R_r at approximately 80 ms. This action results in voltage unbalance across the capacitors, output current distortion, and asymmetrical output voltage levels. Additionally, the capacitor voltages exhibit a transient response of approximately 100 ms. When R_r is disconnected, the voltages across the capacitors converge to $V_{DC}/2 = 40$ V, and the previously observed issues in the output current and voltage are resolved. However, the transient response lasts up to approximately 140 ms, as shown in the capacitor voltage waveforms in Fig. 5.12b.

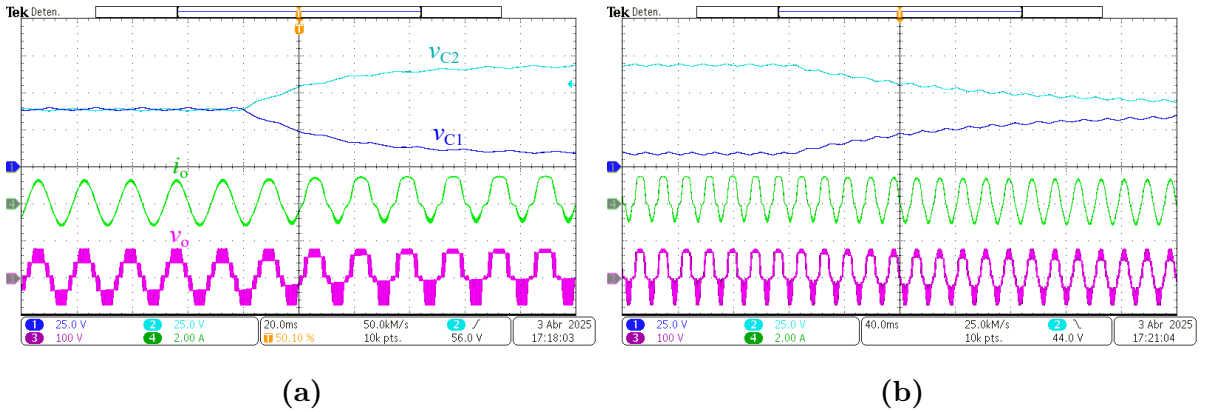


Figure 5.12: Transient states responses of 5L-ATT inverter. In descending order, voltages across C_1 and C_2 (y-axis fixed at 10 V/DIV, x-axis fixed at 10 ms/DIV). The output current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV). The output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV). (a) When R_r is connected, (b) When R_r is disconnected.

5.2.2 Converter and Five-Level Asymmetrical T-Type Inverter both in Open-Loop Operation

The diagram of the 5L-ATT inverter and the converter, considering both converters operating in open-loop mode, is shown in Fig. 5.13. In this test case, the switching signals for the 5L-ATT inverter are generated by the EP4CE22F17C6N FPGA, while those for the converter are generated by the TMS320F28379D DSP.

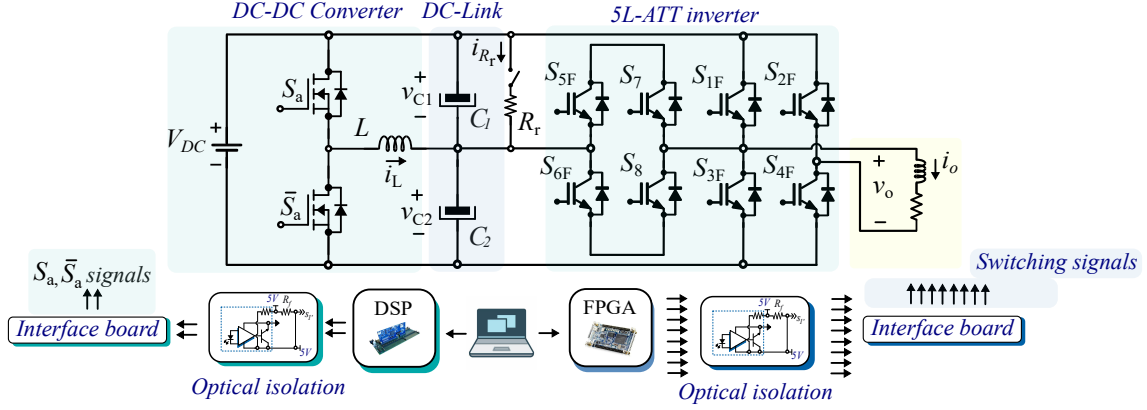


Figure 5.13: Diagram of the 5L-ATT inverter with converter using to experimental validation where the both converters operates in open-loop mode.

Figure 5.14 shows the steady state responses of the voltages across capacitors C_1 and C_2 , as well as the output current and voltage of the 5L-ATT inverter, represented by the blue, cyan, green, and pink waveforms, respectively. These results demonstrate proper voltage balancing of the DC-link in the 5L-ATT inverter. Figure 5.15 presents the same steady state responses; however, the output current waveform is replaced by the current through the inductor L . This inductor current exhibits a grid-frequency AC component, and its peak magnitude corresponds to the inverter output current, superimposed with a ripple due to the switching of the converter.

Figures 5.16 and 5.17 show the transient state responses. Specifically, Fig. 5.16a and Fig. 5.17a show the system behavior when the resistor R_r is connected, while Fig. 5.16b and Fig. 5.17b present the responses after the disconnection of R_r . In Fig. 5.16, the plotted waveforms correspond to the voltages across capacitors C_1 and C_2 , the current through the resistor R_r , i_{R_r} , and the output voltage of the 5L-ATT inverter, represented by the blue, cyan, green, and pink curves, respectively. When the resistor R_r is connected, the transient response lasts approximately 5 ms, and the voltages across the capacitors converge to $v_{C1} = 38$ V and $v_{C2} = 40$ V. Once R_r is disconnected, the voltages across both C_1 and C_2 are restored to 40 V. Figure 5.17 presents the same transient responses as Fig. 5.16, with the difference that the output voltage waveform of the 5L-ATT inverter is replaced by the current through the inductor L . The connection of R_r introduces a negative DC offset in i_L , whose magnitude corresponds to the value of i_{R_r} .

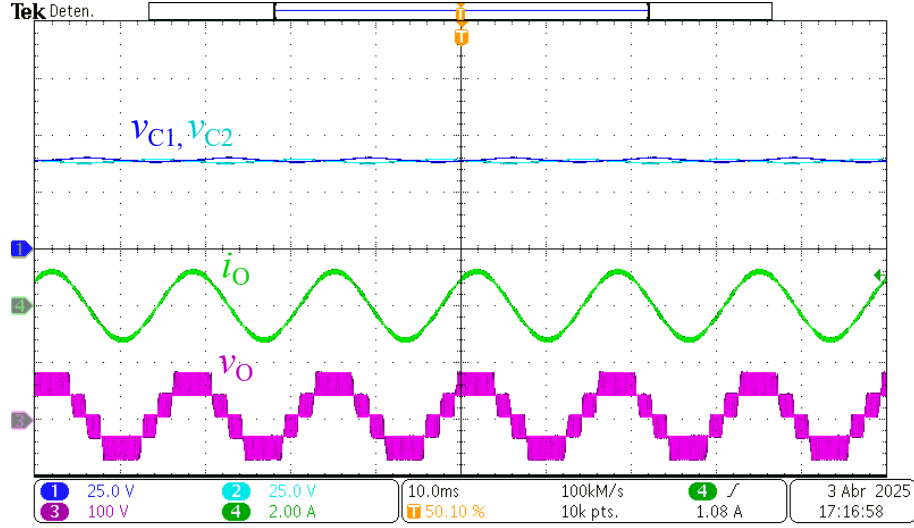


Figure 5.14: Steady states responses of the converter operating in open-loop mode and 5L-ATT inverter. In descending order, voltages across C_1 and C_2 (y-axis fixed at 25 V/DIV, x-axis fixed at 10 ms/DIV), the output current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV).

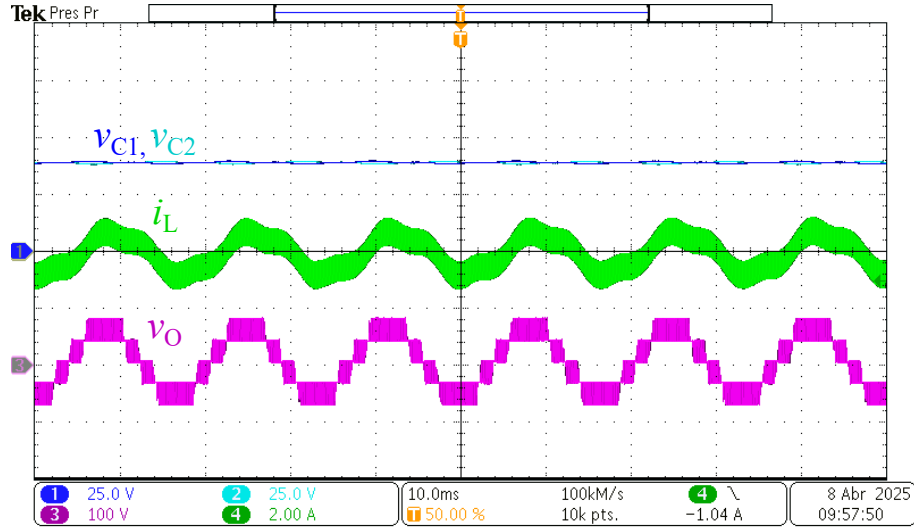


Figure 5.15: Steady states responses of the converter operating in open-loop mode and 5L-ATT inverter. In descending order, voltages across C_1 and C_2 (y-axis fixed at 25 V/DIV, x-axis fixed at 10 ms/DIV). The inductor current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV). The output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV).

5.2.3 Converter in Closed-Loop Together with the Five-Level Asymmetrical T-Type Inverter in Open-Loop

The diagram of the converter operated in closed-loop mode with the 5L-ATT inverter is shown in Fig. 5.18. As a last test case, the switching signals are generated by

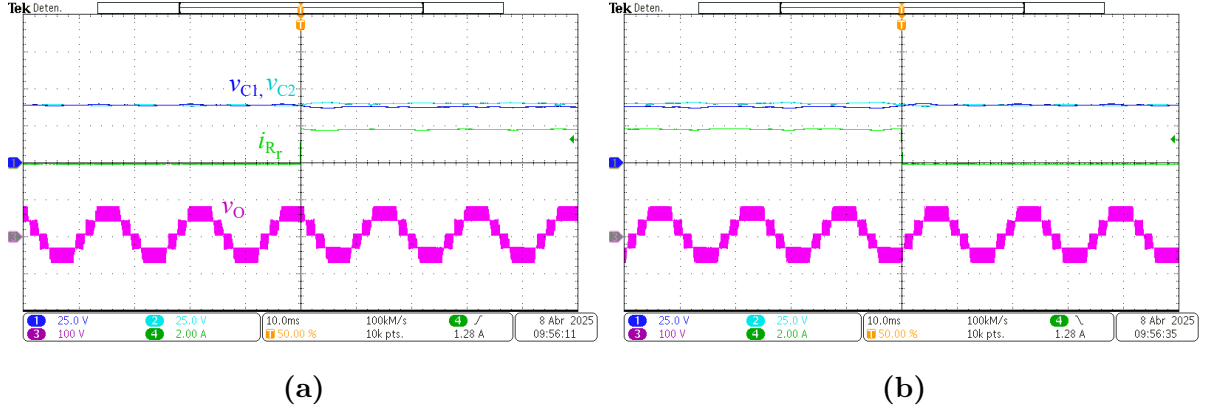


Figure 5.16: Transient states responses of the converter operating in open-loop mode. In descending order, voltages across C_1 and C_2 (y-axis fixed at 10 V/DIV, x-axis fixed at 10 ms/DIV), the current although R_r (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV). (a) When R_r is connected, (b) When R_r is disconnected.

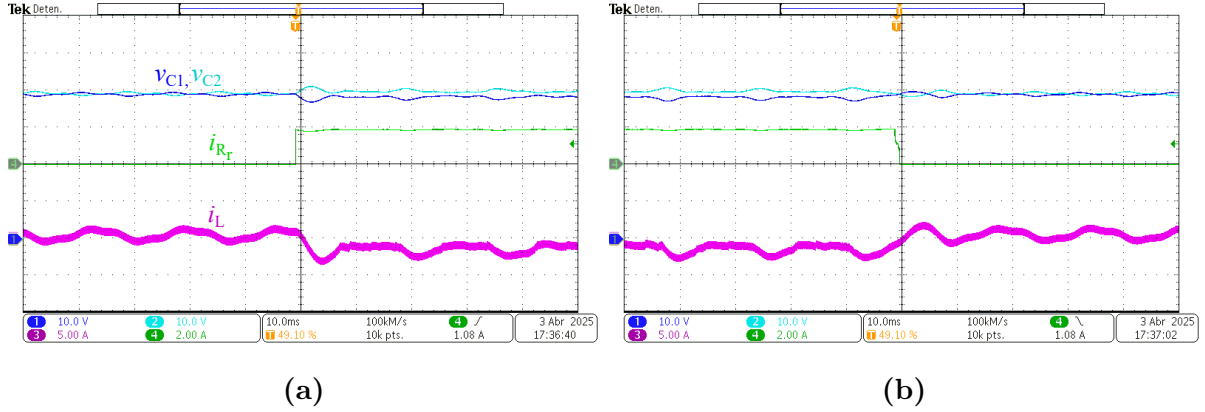


Figure 5.17: Transient states responses of the converter operating in open-loop mode. In descending order, voltages across C_1 and C_2 (y-axis fixed at 10 V/DIV, x-axis fixed at 10 ms/DIV), the current although R_r (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the inductor current (y-axis fixed at 5 A/DIV, x-axis fixed at 10 ms/DIV). (a) When R_r is connected, (b) When R_r is disconnected.

the EP4CE22F17C6N FPGA, and the control scheme proposal is implemented in the TMS320F28379D DSP.

Figures 5.19 and Fig. 5.15 shows the steady-state responses of the both converters. In Figures 5.19 can be shown the voltages across capacitors C_1 and C_2 , as well as the output current and voltage of the 5L-ATT inverter, represented by the blue, cyan, green, and pink waveforms, respectively. On the other hand, Fig. 5.20 presents the same steady state responses; however, the output current waveform is replaced by the current through the inductor L . These results demonstrate the action of the voltage balancing of the DC-link in the 5L-ATT inverter. Additionally, the inductor current exhibits a grid-frequency AC component, and its peak magnitude corresponds to the inverter output current, superimposed with a ripple due to the switching of the converter.

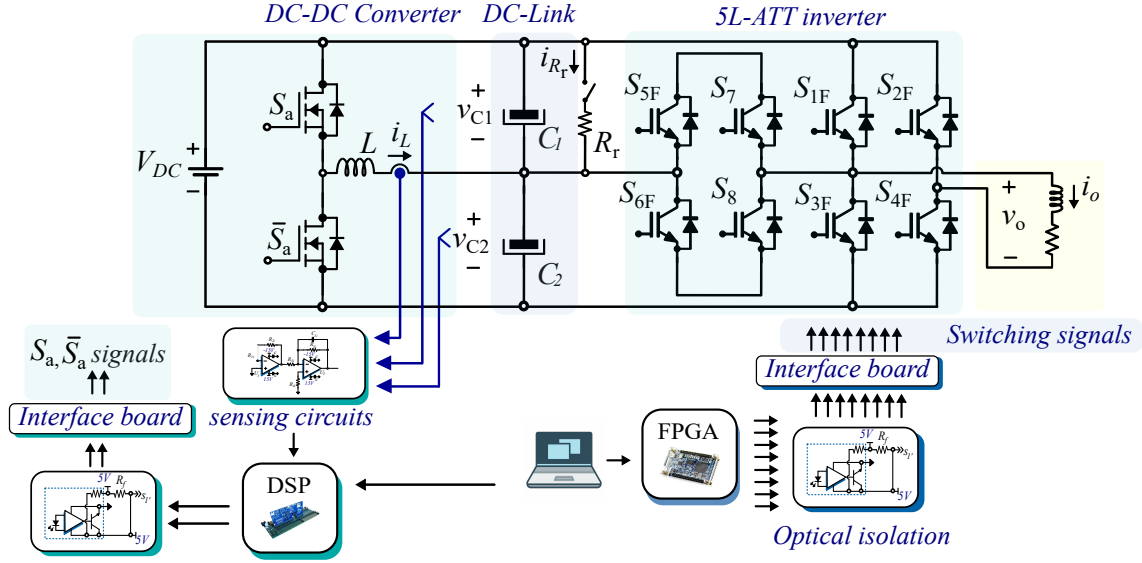


Figure 5.18: Diagram of the 5L-ATT inverter with converter using to experimental validation where converter operate in closed-loop mode.

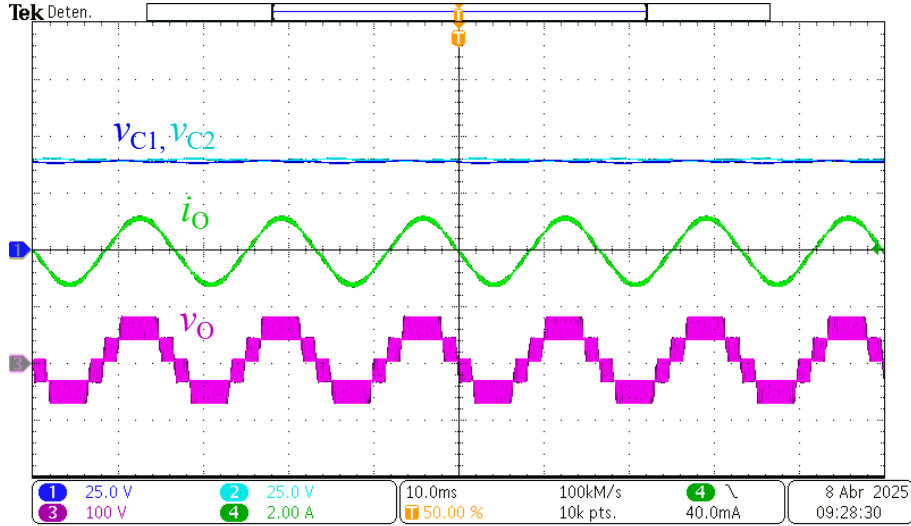


Figure 5.19: Steady states responses of the converter operating in closed-loop mode and 5L-ATT inverter. In descending order, voltages across C_1 and C_2 (y-axis fixed at 25 V/DIV, x-axis fixed at 10 ms/DIV), the output current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV).

Figures 5.21 and 5.22 illustrate the transient behavior of the system. In particular, Fig. 5.21a and Fig. 5.22a correspond to the test case where the resistor R_r is connected, while Fig. 5.21b and Fig. 5.22b show the response when R_r is disconnected. In Fig. 5.21, the waveforms represent the voltages across capacitors C_1 and C_2 , the current flowing through R_r that is denoted as i_{R_r} , and the output voltage of the 5L-ATT inverter, shown in blue, cyan, green, and pink, respectively. When R_r is introduced into the circuit, the capacitor voltages exhibit a transient lasting approximately 3.5 ms, converging to

$v_{C1} = v_{C2} = 40$ V. The output voltage levels of the inverter remain unaffected and maintain their symmetrical behavior. After disconnecting R_r , both capacitor voltages converge to the same voltage 40 V. Figure 5.22 shows the same transient case as Fig. 5.21, with the difference that the output voltage of the inverter is replaced by the current through the inductor L . The connection of R_r causes a negative DC offset in the inductor current i_L , whose amplitude matches that of the current i_{R_r} .

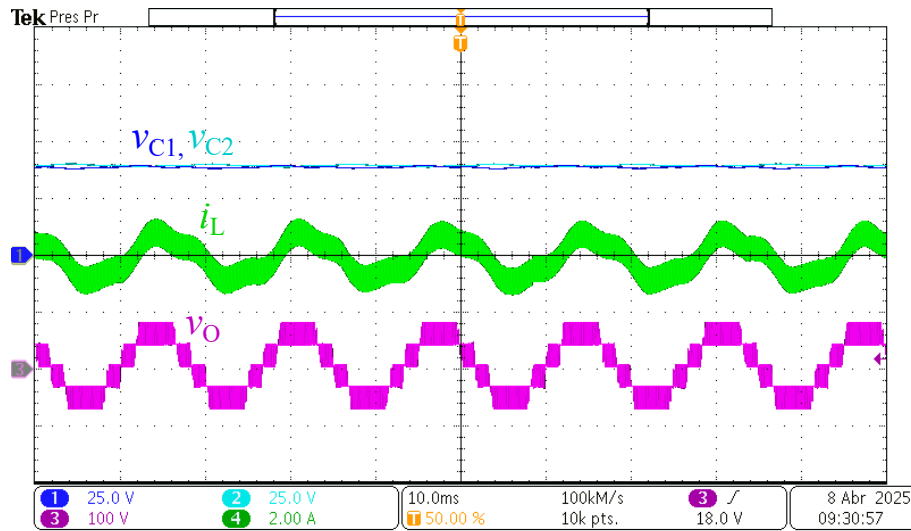


Figure 5.20: Steady states responses of the converter operating in closed-loop mode and 5L-ATT inverter. In descending order, voltages across C_1 and C_2 (y-axis fixed at 25 V/DIV, x-axis fixed at 10 ms/DIV), the inductor current (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV).

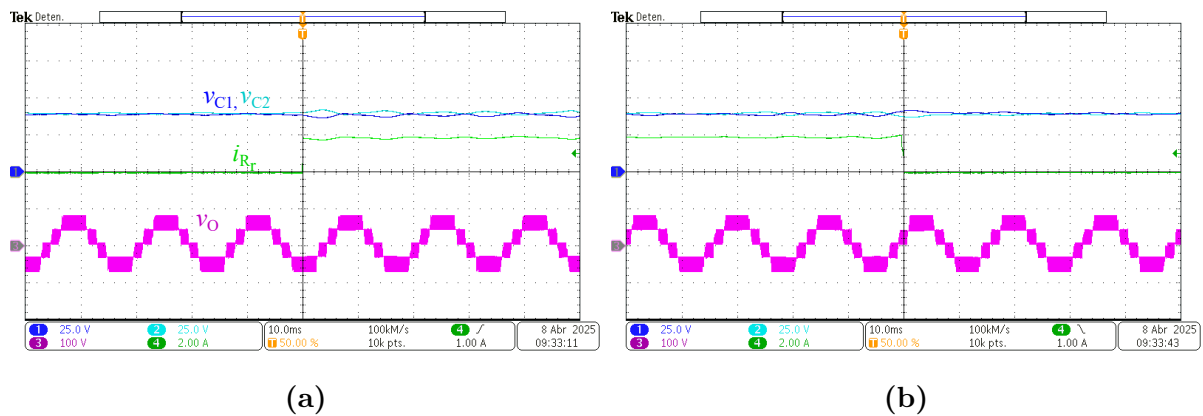


Figure 5.21: Transient states responses of the converter operating in closed-loop mode. In descending order, voltages across C_1 and C_2 (y-axis fixed at 10 V/DIV, x-axis fixed at 10 ms/DIV), the current through R_r (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the output voltage (y-axis fixed at 100 V/DIV, x-axis fixed at 10 ms/DIV). (a) When R_r is connected, (b) When R_r is disconnected.

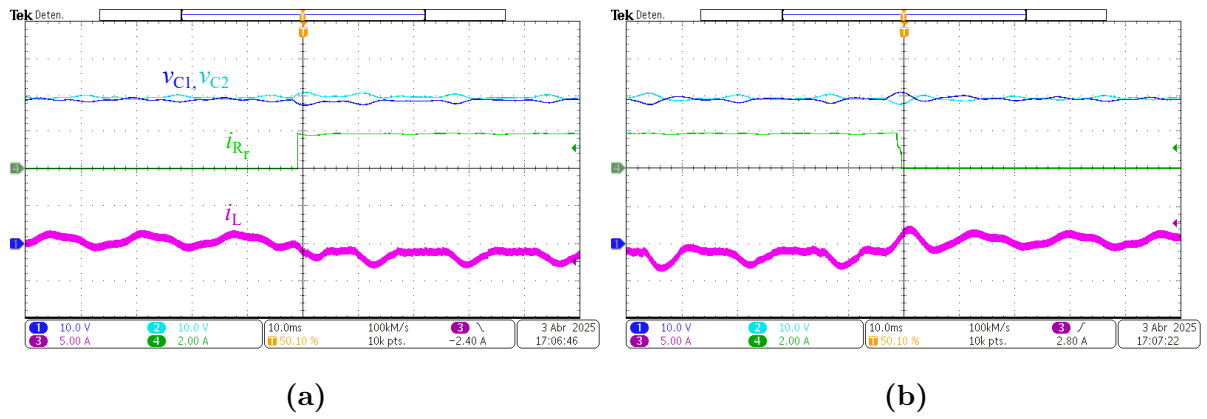


Figure 5.22: Transient states responses of the converter operating in closed-loop mode. In descending order, voltages across C_1 and C_2 (y-axis fixed at 10 V/DIV, x-axis fixed at 10 ms/DIV), the current although R_r (y-axis fixed at 2 A/DIV, x-axis fixed at 10 ms/DIV), the inductor current (y-axis fixed at 5 A/DIV, x-axis fixed at 10 ms/DIV). (a) When R_r is connected, (b) When R_r is disconnected.

Chapter 6

Conclusions

This thesis presented the study, analysis, control proposal, and implementation of a DC-DC converter aimed at regulating the voltages across two DC-link capacitors in a multilevel inverter. The converter analysis included volt-second balance on the inductor and charge balance on the output capacitor, in continuous conduction mode, to obtain the steady-state operating parameters. In addition, an averaged state-space model was derived to evaluate closed-loop stability using the Routh-Hurwitz criterion.

The main control objective was to regulate the voltage imbalance between the DC-link capacitors. The proposed control structure included an outer loop to regulate the voltage difference using a proportional-integral controller, and an inner loop to regulate the inductor current using a proportional controller. The multilevel inverter used in this thesis was a five-level asymmetric T-type inverter. Its operating principle and modulation scheme, based on level-shifting and phase disposition PWM, were also presented.

The results confirmed closed-loop stability for a range of controller gain values. Furthermore, numerical validation of the DC-link voltage balance performance was performed in three different operating configurations. First, the five-level asymmetric T-type inverter was tested for open-loop operation with equal DC-link capacitors, and then under a simulated abnormal condition by connecting a resistor in parallel with one of the capacitors. The same scenarios were tested again in a configuration where the converter was connected between the DC voltage source and the DC-link capacitors in open-loop mode. Finally, the tests were repeated with the converter operating in closed-loop mode.

The implementation involved the design, construction, and experimental validation of laboratory prototypes of both the converter and the five-level asymmetric T-type inverter. The experimental setup included a voltage-sensing circuit, a current-sensing circuit, an interface board that drives the power converters, and the converter and inverter hardware. The control algorithm was implemented on a Texas Instruments Delfino TMS320F28379D DSP board and programmed to operate in real time. The modulation scheme was generated using an Altera Cyclone IV FPGA on the DE0-Nano development board.

The experimental tests replicated the same operating conditions used in the numerical validation. In both cases, the proposed control method was validated, demonstrating a fast dynamic response and reliable performance under all test conditions. An advantage of the converter proposed in these experimental tests is its ability to operate independently of the inverter topology, making it a modular solution. Furthermore, its structure is simple, consisting only of two power switches and an inductor. However, it is important to emphasize that this inductor must have similar electrical characteristics to those of the inductor used in the multilevel inverter.

Future works:

- Evaluate the efficiency of the DC-DC converter analyzed in this thesis.
- Perform numerical and experimental validation of the converter using different multilevel inverter topologies.
- Analyze and propose a control scheme for the DC-DC converters presented in [2,63]. The control objective remains the same: regulating the DC-link voltage across two capacitors.
- Compare the dynamic responses of each converter, both with and without the control scheme proposed.

LIST OF PUBLICATIONS

- D. G. Castañeda-Rubalcaba, J. M. Sosa, G. Vázquez-Guzmán and P. R. Martinez-Rodriguez, "Brief Overview on Non-Isolated DC-DC Bidirectional Power Converter Topologies," 2023 IEEE International Autumn Meeting on Power, Electronics and Computing (ROPEC), Ixtapa, Mexico, 2023, pp. 1-6, doi: 10.1109/ROPEC58757.2023.10409457.
- D. G. Castañeda-Rubalcaba, J. M. Sosa, G. Vázquez-Guzmán and V. H. Compeán-Jasso, "Experimental Validation of a Non-Isolated DC-DC Bidirectional SEPIC," 2023 International Symposium on Electromobility (ISEM), Monterrey, Mexico, 2023, pp. 1-7, doi: 10.1109/ISEM59023.2023.10334769.
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