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ANALYSIS OF A TRANSFORMERLESS CHB CONVERTER WITH LEAKAGE CURRENT COMPENSATION

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PRESENTA:

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se autoriza la impresión de la tesis titulada "Análisis de un convertidor CHB sin transformador con compensación de corrientes de fuga" realizada por el estudiante **C. Juan Antonio Verdin Cruz** con número de control **IP20110056** la cual ha sido desarrollada dentro del programa de la Maestría en Ingeniería Electrónica bajo la dirección del Dr. Gerardo Vázquez Guzmán y la codirección del Dr. Pánfilo Raymundo Martínez Rodríguez y ha sido revisada y aprobada por el comité tutorial antes mencionado.

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Constancia de aprobación de la tesis

La tesis **Analysis of a transformerless CHB converter with leakage current compensation** presentada para obtener el Grado de Maestro en Ingeniería Electrónica fue elaborada por el **Ing. Juan Antonio Verdin Cruz** y aprobada el **07 de julio de 2022** por los suscritos, designados por el Consejo de Posgrado de la Maestría en Ingeniería Electrónica del Tecnológico Nacional de México / Instituto Tecnológico Superior de Irapuato.

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El proyecto de tesis titulado “Analysis of a transformerless CHB converter with leakage current compensation” fue desarrollado e implementado dentro de las instalaciones del Instituto Tecnológico Superior de Irapuato bajo la dirección del Dr. Gerardo Vázquez Guzmán y del Dr. Pánfilo Raymundo Martínez Rodríguez, así como de la asesoría del Dr. José Miguel Sosa Zúñiga y del Dr. Mario Alberto Juárez Balderas. La implementación experimental tuvo lugar dentro del Laboratorio de Electrónica de Potencia, el cual cuenta con el equipamiento adecuado para la culminación del proyecto antes mencionado. Cabe señalar que además de utilizar el equipo de laboratorio para desarrollar el prototipo electrónico, se hace uso de bases teóricas como libros, manuales, entre otros documentos técnicos, los cuales son fundamentales para el sustento matemático del proyecto de tesis. Esta información fue proporciona a través del departamento de biblioteca y de sus plataformas digitales.

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Juan Antonio Verdin Cruz, Irapuato, Guanajuato, México, julio de 2022.

CONTENTS

ABSTRACT

Nowadays, the development of new inverter topologies have been growing up since the global electric demand requires an efficient conversion ratio. In the state of the art several topologies for photovoltaic applications have been presented which address different specific issues, however, the requirements for energy quality, manufacturing costs and weight have not still been achieved. Currently, it is well known that multilevel inverters have gained popularity within the energy market as well as for many researchers because of their proficient characteristics such as: being suitable for high power applications, less filtering requirements and electrical stress on devices, low harmonic content even if the converter is operated at low frequency, fault tolerant operation and high electromagnetic compatibility. On the other hand, one alternative to reach a high efficiency is by eliminating the transformer of the photovoltaic system tied to the utility grid. This system is called transformerless system whose structure is based on the DC-AC converter and the low pass filter connected to the grid. As was previously mentioned transformerless systems are preferred for PV applications, however, the leakage ground current drawback arises in this kind of system. This phenomenon is caused by the parasitic elements on the photovoltaic module which are related with the mechanical structure, installation and environmental conditions. The parasitic elements are called parasitic capacitances and when a transformerless photovoltaic system is connected to the grid, these capacitances provide a trajectory for the leakage current to flow through the ground path. The leakage current mostly depends on inverter common mode voltage, therefore, a varying common mode voltage produces high leakage currents. In addition, the common mode voltage is produced by the switching sequence of the power semiconductors of the converter. Several techniques are introduced to compensate the leakage current, although, these can be classified in three global types which are: modulation schemes, reconfiguration of the converter structure, and passive filters. In this work an deeply analysis of the leakage current issue and the three methods to mitigate this phenomenon are presented. Moreover, a solution to the leakage ground current issue for the cascaded H-bridge converter is based on passive filter design is proposed, in addition, the common and differential mode models of the proposed structure is obtained to provide a better understanding of the leakage current behav-

ior. The proposed topology is evaluated by the classical modulations scheme (level-shifted and phase-shifted PWM) to compare the output response in terms of leakage current, efficiency and harmonic content. 1 kW laboratory prototype is implemented to experimentally assess the proposed filter. Finally, the results are validate with the international standard DIN VDE 0126-1-1 which imposes a limit of 300 mA as maximum leakage current.

RESUMEN

Actualmente el desarrollo de nuevas topologías inversoras se ha incrementado debido a que se requiere una mayor eficiencia en conversión de energía para abastecer la demanda eléctrica global. La literatura ha presentado diferentes topologías CD-CA para aplicaciones en sistemas fotovoltaicos, las cuales abordan ciertos problemas en específico, sin embargo, los requerimientos de calidad de la energía, costos de manufactura y tamaño aun no se ha logrado efectivamente. Hoy en día, los convertidores multinivel han ganado popularidad dentro del mercado energético asi como para los investigadores debido a sus excelentes características las cuales son: adecuado para alta potencia, menor requerimiento de filtrado, alta eficiencia, menor estrés eléctrico en los interruptores de potencias, entre otros. Por otro lado, una de las alternativas para lograr una alta eficiencia es mediante la eliminación del transformador del sistema fotovoltaico con conexión a la red eléctrica al cual se refieren como sistema sin transformador cuya estructura se basa en un convertidor CD-CA y un filtro pasa bajas conectado a la red. Como se menciono anteriormente, los sistemas sin transformador se prefieren en aplicaciones fotovoltaicas, sin embargo, surge el problema de corriente de fuga en este tipos de sistemas. Este fenómeno es denominado como capacitancias parásitas y está relacionado directamente con la construcción mecánica, la instalación y las condiciones ambientales. Al tener un sistema fotovoltaico no aislado conectado a la red, se crea una trayectoria entre las capacitancias parásitas y la conexión a tierra del sistema, permitiendo el flujo de corrientes de fuga. Mayormente, la corriente de fuga está relacionada con el voltaje de modo común del convertidor, por tanto, se producirá una corriente de fuga si se tienen variaciones en el voltaje de modo común. Estas variaciones son estimuladas por la secuencia de conmutación de los interruptores de potencia del convertidor. Dentro del estado del arte se han reportado algunas soluciones para compensar el problema de corrientes de fuga y estas se pueden clasificar en tres principales tipos: diseño de esquemas de modulación, reconfiguración de la topología CD-CA y mediante filtros pasivos. En este proyecto de tesis se presenta una solución para la corriente de fuga basada en el diseño de filtro pasivo. Además, se presenta el modelo de modo común y diferencial para una mejor comprensión de la solución propuesta. La topología propuesta es evaluada con los principales esquemas de modulación (modulación

por ancho de pulso desplazada en nivel y en fase) y se obtienen resultados numéricos a través del software de simulación PSim y experimentales mediante la implementación de un prototipo experimental de 1kW. Por otro lado, mediante la utilización de modelos térmicos, se obtiene una tabla comparativa de eficiencia de la topología propuesta bajo las secuencias de conmutación implementadas. Los resultados obtenidos son validados a través del estándar internacional DIN VDE 0126-1-1 que impone como límite máximo una corriente de fuga de 300 mA, la cual se logra mediante la conexión del filtro diseñado.

NOTATION

Common acronyms

DC	Direct Current
AC	Alternating Current
ADC	Analog-to-Digital Converter
IGBT	Isolated Gate Bipolar Transistor
PV	Photovoltaic
TL	Transformerless
LFT	Low Frequency Transformer
HFT	High Frequency Transformer
NPC	Neutral Point Clamped
FC	Flying Capacitor
CMI	Cascaded Multilevel Inverter
CHB	Cascaded H-Bridge
LGC	Leakage Ground Current
CM	Common Mode
DM	Differential Mode
CMC	Common Mode Current
CMV	Common Mode Voltage
DMV	Differential Mode Voltage
DMC	Differential Mode Current
IPD	In-Phase Disposition
POD	Phase Opposite Disposition
APOD	Alternative Phase Opposite Disposition
PSPWM	Phase-Shifted
LSPWM	Level-shifted

LIST OF FIGURES

1. INTRODUCTION.

1.1 Photovoltaic systems

The electric demand is a common issue in whole world as the world population rise. Besides, the fossil fuels as electric energy source represents an important challenge because they are not guaranteed for near future. In addition, the pollution has increased due to the emission of carbon dioxide (CO_2). Thus, the researches have focused on the technological development with the purpose to take advantage of the renewable resources as alternative way to energy generation. In recent decades, the renewable energies have taken an important role supplying the electrical energy. Among the renewable energy, the most common types are the following: wind energy, solar energy, hydraulic energy, geothermal energy, and biomass energy. Sunlight is one of the most abundant and freely available natural resource over almost world regions. In recent years, electric generation through photovoltaic (PV) systems has been the fastest growing source of power generation worldwide. The increase in solar plants in Mexico according to Centro Nacional de Control de Energía (CENACE) has been greater than wind power plants. Comparing the trend of December 2019 to December 2020 the solar plants increased by 40% whereas the wind plants was by 33%. In photovoltaic power plants, the global installed photovoltaic capacity for 2020 has been 775 GW as it can be observed in the Fig. 1.1 [1]. Among the combined markets formed by North and South America, 25 GW have been added in 2020 to obtain 120 GW as a total cumulative power. The largest markets in 2020 are represented by U.S. (19 GW), Brazil (3.9 GW) and Mexico (1.5 GW). The clean energy utilization represents an attractive market in Mexico due to the benefits in terms of projects development. The current outlook is

described as follows [2],

- 6,574 MW installed capacity divided into large-scale and distributed solar generation.
- +$9,100 MUSD direct investment.
- +85% of the national territory optimal for solar projects.
- Solar technology costs have been reduced by up to 73% .

An overview of the solar power plants distributed in Mexico is depicted in Fig. 1.2. Notice that most of the territory is suitable to implement solar projects. In other matters, the PV systems can be classified into three main groups, nevertheless, these systems are explained in the next section.

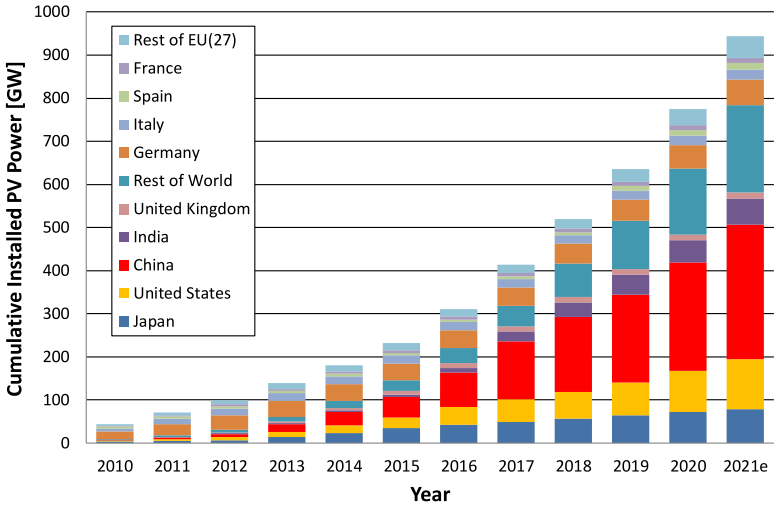

Fig. 1.1: Cumulative installed photovoltaic power worldwide [1].

1.2 Types of photovoltaic systems

As can be shown in Fig. 1.3 a PV system is formed by connecting an array of photovoltaic modules and a power converter in order to obtain a suitable current to supply different loads [4]. Normally, the power conversion is carried out by a DC-AC converter or inverter. Among the PV systems, there are three groups which are classified according to their function and how they are connected with the other electric devices, for instance, how the system is interfaced with the utility grid. This classification is listed below [5], [6],

Fig. 1.2: Solar plants distribution in Mexico (72 solar plants in commercial operation, April 2021) [2].

- Stand-alone systems.
- Grid tied systems.
- Hybrid PV systems.

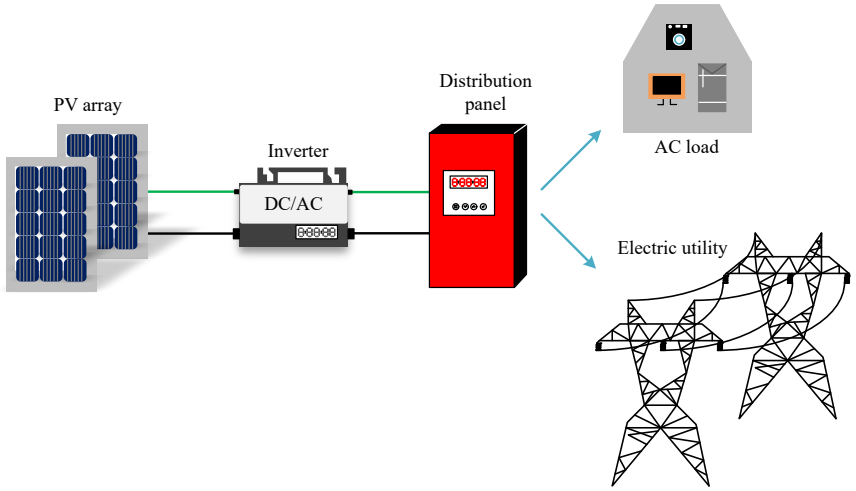

Fig. 1.3: Grid connected PV system.

The stand-alone PV system is designed to operated with no electric utility grid connection, which makes it an excellent alternative in areas where there is no access to the utility grid. This system uses batteries as an energy storage of the energy generated by the solar panel and the DC-AC loads are feeding by means of the batteries. On the other hand, solar energy depends mostly on climatic conditions, thus to operate at the maximum power point of the solar panel, a DC-DC converter is used. The diagram of this system is illustrated in the Fig. 1.4.

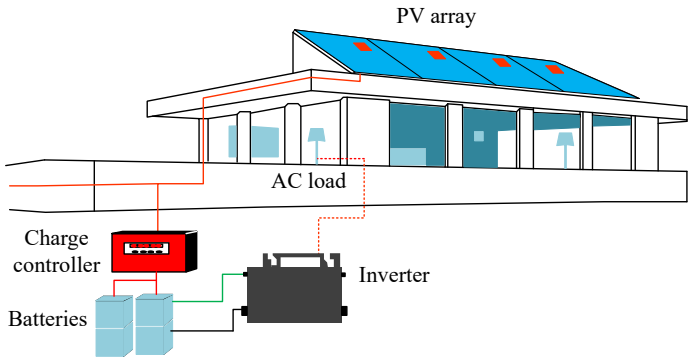

Fig. 1.4: Stand-alone PV system.

Grid tied PV systems is able to inject power to the grid with the desirable characteristics such that power quality and safety standards. The primary electronic device is the inverter, which has to convert DC energy to AC energy with the voltage and power quality requirements demanded by the electric utility grid. The configuration of the latter PV system is similar to the Fig. 1.3. A hybrid system consists of several sources feeding a common DC bus or AC loads, for example, it can use utility power, wind or solar energy as an auxiliary source as it can be observed in Fig. 1.5. Normally, this type of system is designed and sized for powering a certain DC/AC loads, for example: water pumps, lighthouses, telecommunication repeater stations, among others.

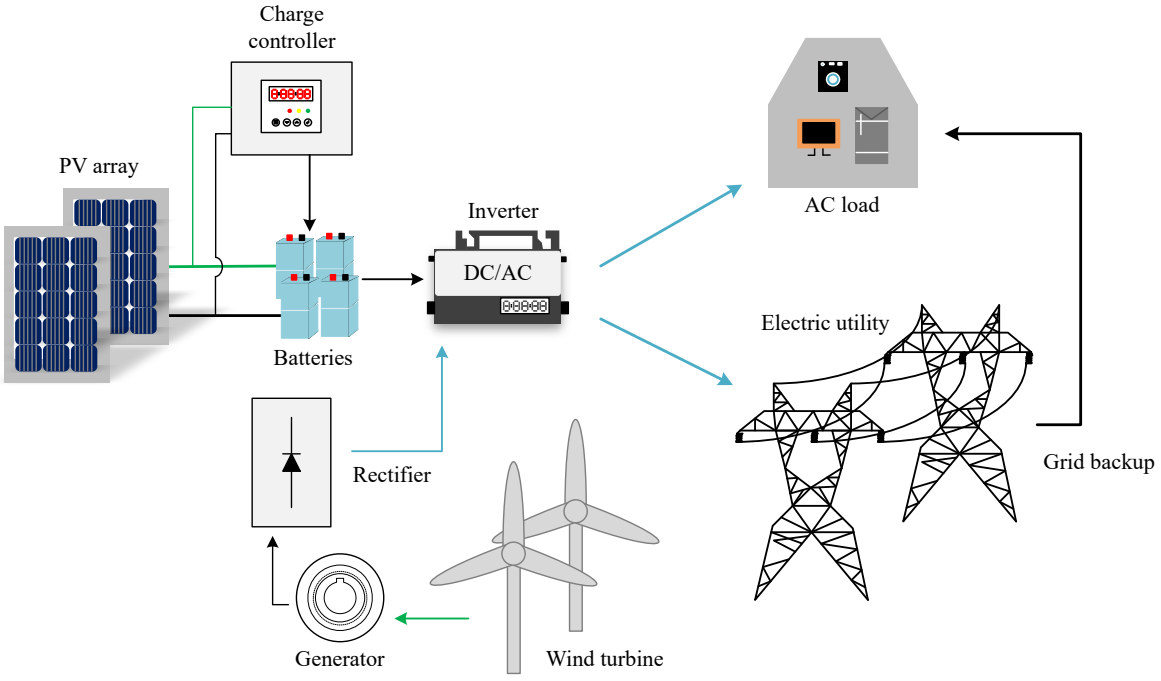

Fig. 1.5: Hybrid PV system configuration.

Due to the modularity of the PV arrays, they allow designing several configurations for a specific application. Nevertheless, these can be reorganized according to power rate and the connection of the electric devices. In the Fig. 1.6 the configurations between the PV array and the inverter are shown [3], [7], [8]. For a power rate less than 300 W, the configuration represented in Fig. 1.6 (a) is commonly used. This type of connection is known as microinverter or integrated module. Another alternative is the string inverter configuration which is illustrated in Fig. 1.6 (b), this alternative consists of arranging PV arrays in order to divide the power (3 kW to 5 kW) and use a single inverter per array. String inverters allow improving the system efficiency and reduce the mismatch losses. A new configuration arise based on string inverter and it is called as multi-string inverter, this topology uses several arrays of PV modules and DC-DC converters, each converter is connected to the utility grid by a single inverter. The benefits of this configuration are: reduction of the voltage level required in the PV array terminals, and high efficiency similar to the string configuration, this topology is depicted in Fig. 1.6 (c). The most common configuration is the central inverter which is shown in Fig. 1.6 (d). The central inverter is used in applications that required more than 10 kW. All the PV arrays are connected to the central inverter. The key features are: high efficiency and a lower cost per kilowatt generated. Although, this configuration suffers from power losses in cases of mismatch losses and partial shading.

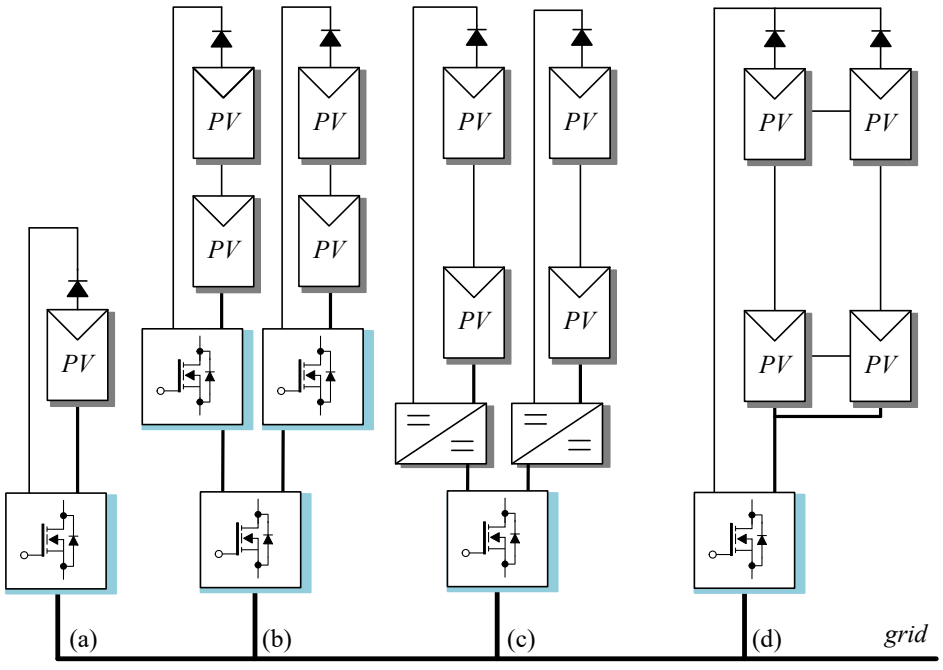

Fig. 1.6: Classification of the inverter tied to utility grid: (a) microinverter, (b) string inverter, (c) multi-string inverter and (d) central inverter.

Several configurations has been studied and presented for PV applications, however, it is possible to classify according to the grid connection interface, in this case, the literature report two types of PV systems tied to the grid which are isolated and non-isolated or transformerless (TL) systems [7], [8]. These kind of interfaces are depicted in Fig. 1.7 and Fig. 1.8 respectively. The isolated system is classified as follows.

- Line-frequency isolated structure: in this case the PV system includes a transformer at the AC side which helps to prevent the flow of DC components into the grid and creates a galvanic isolation between the converter and the utility grid, also, this type of PV system ensures the personal safety standards. Nevertheless, it has a bulky transformer, high costs and lower efficiency (efficiency conversion from 94 to 96%).
- High-frequency isolated structure: this is a multi-stage converter which is recommended for low and medium-power, the transformer has a lower size, however, power losses are increased (efficiency conversion from 90 to 95%). This kind of structure has three configuration: DC-link form, pseudo DC-link form, and without DC-link form.

A TL system is a better alternative where the efficiency is a key parameter, this type has been implemented in recent years due to its features. Some advantages of this structure are: high efficiency, reduced costs and weight. Normally the system is based on a single-stage or two-stage. In two-stage TL systems, the first stage includes a DC-DC converter to adequate the input voltage of the post-stage (inverter-stage). However, a single-stage TL system has higher efficiency but it requires a higher input voltage from PV modules regarding to peak voltage of the grid [9]. A remarkable advantage of both TL systems is the connection with the grid, notice that a low pass filter is only required which represents less power losses. According to the mentioned characteristics of the TL systems, these inverters are becoming the preferred structure for inverter design companies as well as researchers.

1.3 DC-AC multilevel converters

Addressing the types of DC-AC converters, it can be enlisted in the following classifications: two and three level inverters and multilevel inverters. The Fig. 1.9 shows the operating principle of the two, three and multilevel converters. As can be observed, the voltage levels are defined by voltage sources based on capacitors, that is, the voltage level is obtained by switching among the

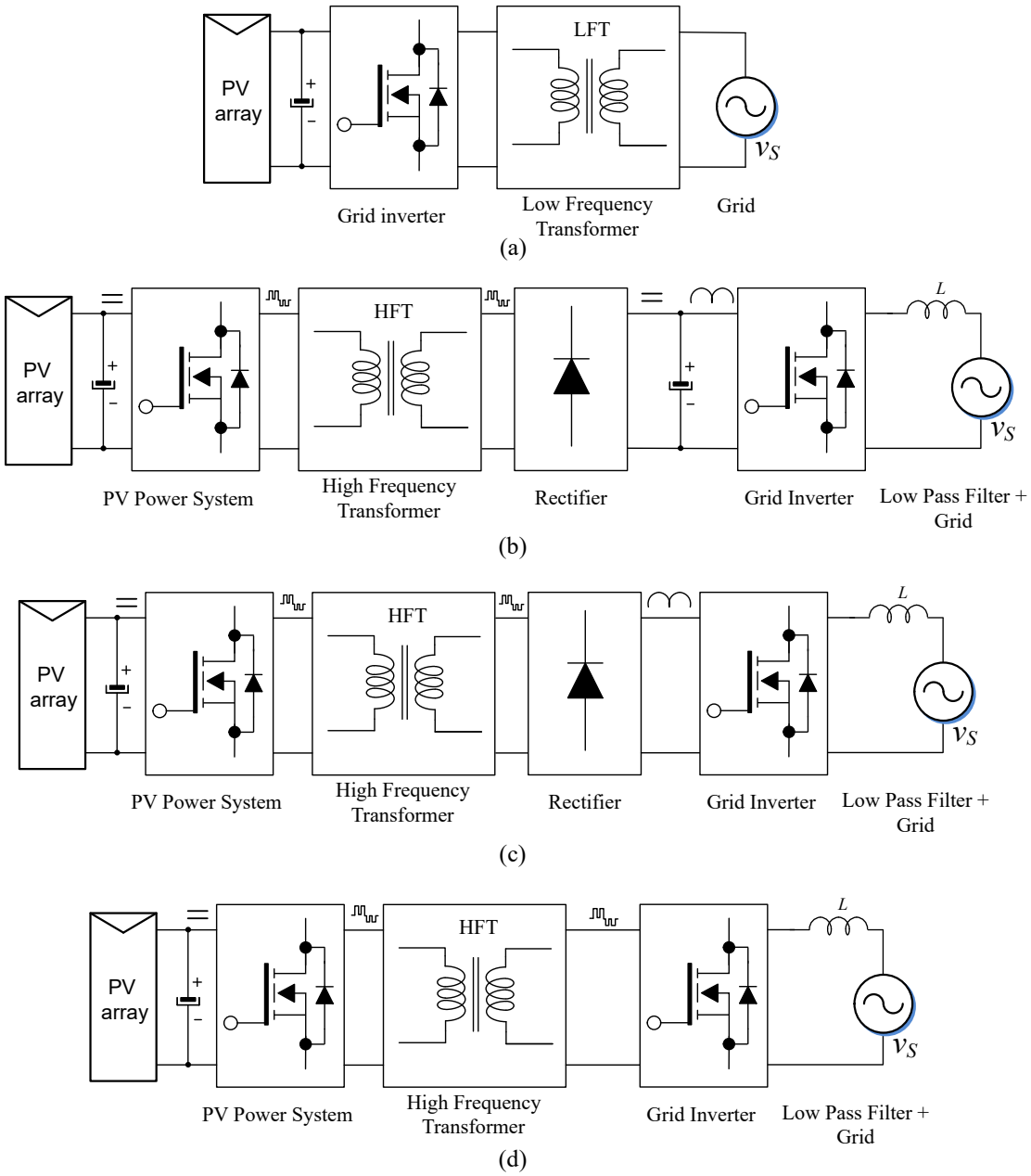

Fig. 1.7: Isolate grid tied PV systems: (a) line-frequency structure, (b) high-frequency structure with DC-link, (c) high-frequency with pseudo DC-link and (d) high-frequency without DC-link.

terminal of each capacitor [11]. For instance, in Fig. 1.9 (a) there are only two levels, the first one is determined by connecting the output at the positive terminal of the capacitor, whereas, the second level is obtained by switching the output to the negative terminal of the capacitor. Following this principle, in Fig. 1.9 (b) three levels are available, in this case, the zero voltage is set by switching the output to the neutral point of the capacitors. Finally, with the purpose to synthesize a stepped voltage waveform at the output, several DC sources are required to set

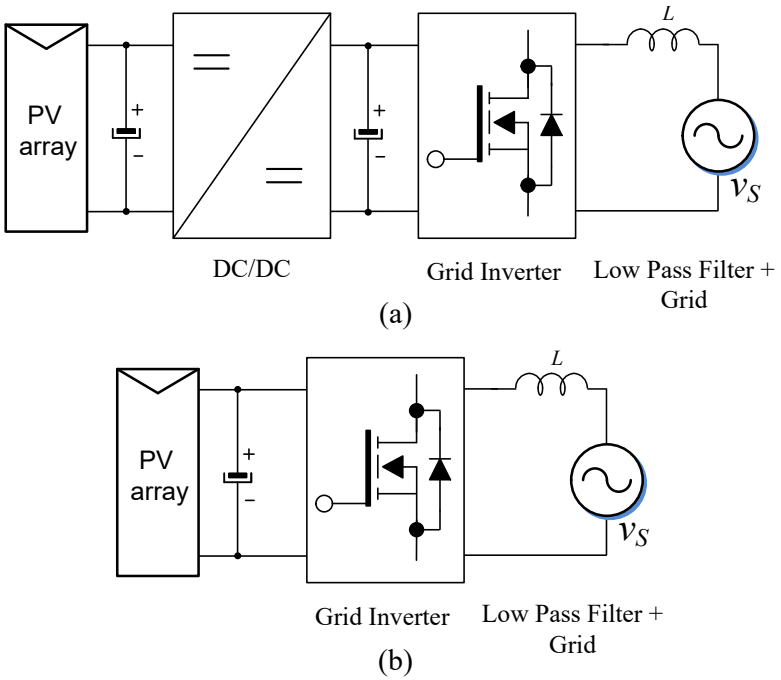

Fig. 1.8: Non-isolate grid tied PV systems: (a) single-stage and (b) two-stage structure.

the different voltage levels at the inverter output as shown in Fig. 1.9 (c). Analysing the topologies before mentioned, multilevel converters represents a promising alternative for high power applications due to its features. Some of the well known advantages are: less dv/dt variations and harmonic distortion in output voltage and current, it can be operated at lower switching frequency, reduces the electrical stress on devices since it generates lower common mode voltages, high electromagnetic compatibility, high power and fault tolerant operation [11], [12]. Taking into account these features, multilevel converters are widely spread in many applications such as: distribution static synchronous compensator (D-STATCOM), high voltage DC transmission (HVDC), pumps, conveyors, motor drives, fans and flexible AC transmission system (FACTS) [13], [14]. In recent decades, many topologies have been developed to meet the requirements of several specific applications which are commercially available. A multilevel topologies classification is shown in Fig. 1.10 [10]. Notice that, there are three essential topologies which are: diode clamped or mostly called neutral point clamped (NPC), flying capacitors (FC) and cascaded multilevel inverter (CMI), these topologies are depicted in Fig. 1.11 [15]. NPC topology is a structure based on clamping diodes as can be seen in Fig. 1.11 (a). The number of diodes,

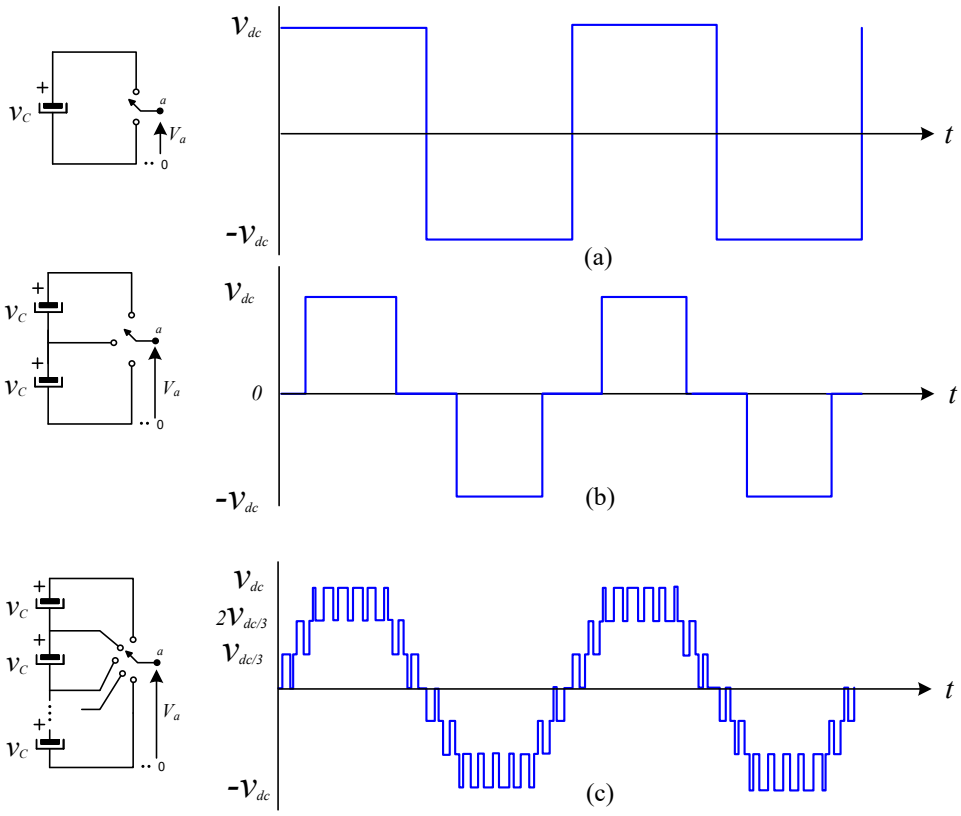

Fig. 1.9: Operating principle: (a) two-level voltage inverter, (b) three-level voltage inverter and (c) multilevel inverter.

power switches and DC sources (capacitors) of this structure is defined as:

$$\begin{aligned} N_{ps} &= 2(m-1) \\ DC_s &= m-1 \\ N_d &= (m-1)(m-2) \end{aligned}$$

where m is the number of voltage levels, N_{ps} is the number of power switches, DC_s is the number of capacitors and N_d is the number of diodes. Some advantages of this topology are: voltage across the power switches is half of the DC source, voltage harmonic content is set on twice of the switching frequency, used on back to back inverters, high efficiency at low frequency. However, a large number of high speed diodes is required for m-level and control methodology is complex, besides, a series connection of clamping diodes is required for high power applications. Flying capacitor (FC) inverter is similar to NPC, this structure is based on capacitors to limit the voltage and obtain each voltage level by switching among each branch of capacitors. The advantages of this topology are: reduce dv/dt stress, clamping diodes are eliminated. Some drawbacks are: low reliability, expensive, complex control scheme for balancing the voltage

across the capacitors and start-up. The number of power switches and capacitors for m-level are the same than the NPC structure. The cascaded H-bridge (CHB) is the most common of the cascaded converter topologies. This converter is a series connection structure, that is, there are n power cells connected. for m-level requires $N_{ps} = 2(m-1)$, DC bus capacitors are equal to $DC_s = (m-1)/2$. CHB provides some advantages regarding NPC and FC converter since it is more flexible converter (easy packaging and storage), less components are required for the start-up which represents a low cost, in addition, the voltage unbalancing among the power cells is very small. Nevertheless, separate DC sources are needed for each power cell.

In this work an analysis of CHB is performed since it provides a simple circuit which offers high efficiency, low cost, a large number of modulations and reliability according to the proficient characteristics explained above for each multilevel topology.

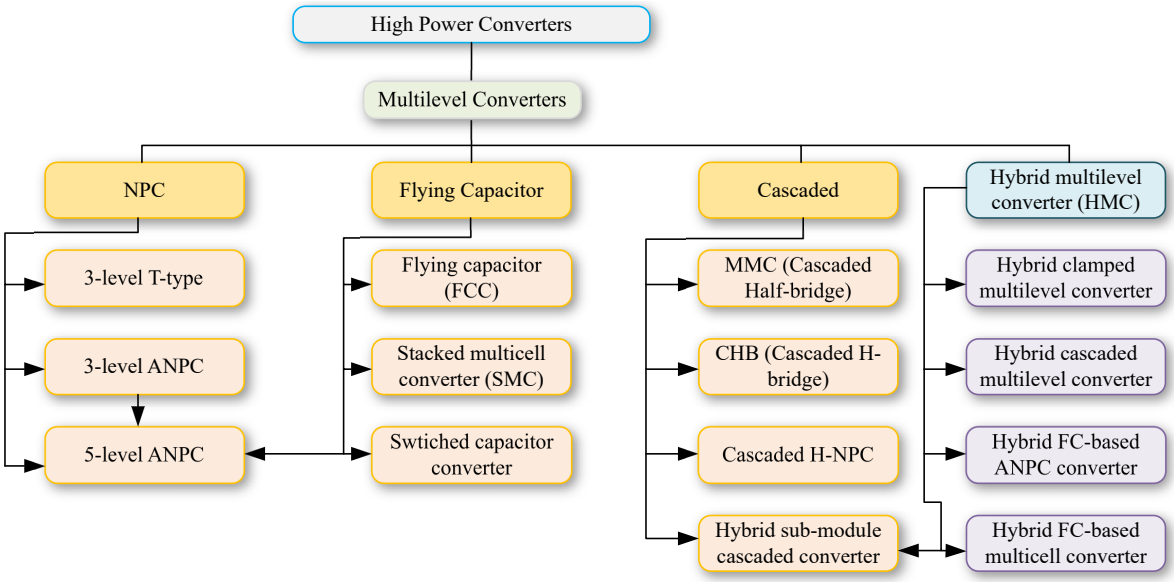

Fig. 1.10: Multilevel converters classification.

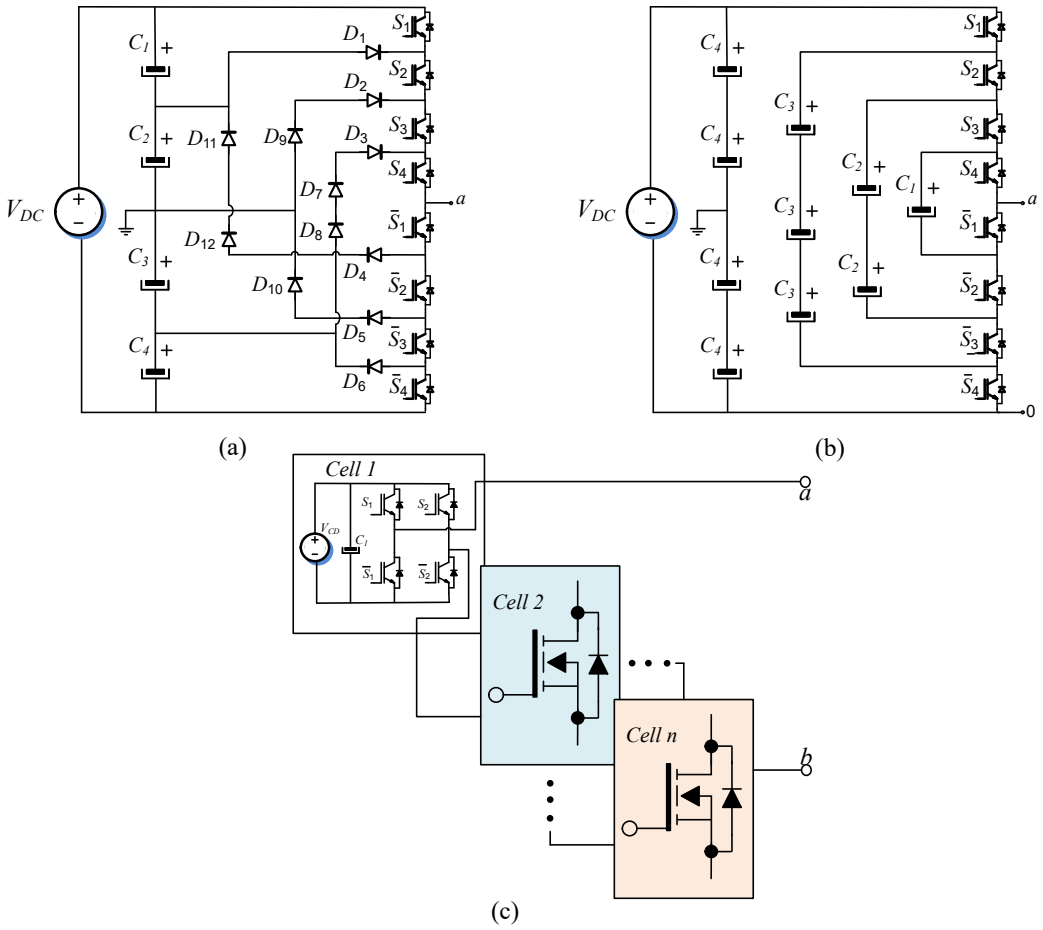

Fig. 1.11: Basic multilevel structure: (a) NPC, (b) FC and (c) CMI.

1.4 Leakage currents

Using a TL system represents high efficiency, low cost and weight, nevertheless, an issue is introduced when the transformer is eliminated. Normally this phenomenon is called leakage ground current (LGC). For a better understanding of this issue, in this section a deeply analysis is presented. LGC is produced by the stray capacitances of the PV module. Normally, the PV modules exhibit capacitance according to the design, the mechanical structure and their installation. Consequently, the capacitances increase considerably in a large number of connected PV modules. A PV module structure is illustrated in Fig. 1.12, where C_1, C_2 and C_3 are the capacitances due to the film of water on the glass, the grounded frame and the roof surface area. An arrangement of this PV module creates an electrical conductor where the charge is stored when the PV system is operated. Since these capacitances are considered as a undesirable side-effect, normally these

are referred as stray capacitances whose expression is defined as $C_{PE} = C_1 + C_2 + C_3$ [16]. In a TL system tied to the grid, the capacitances play an important role as generators of LGC.

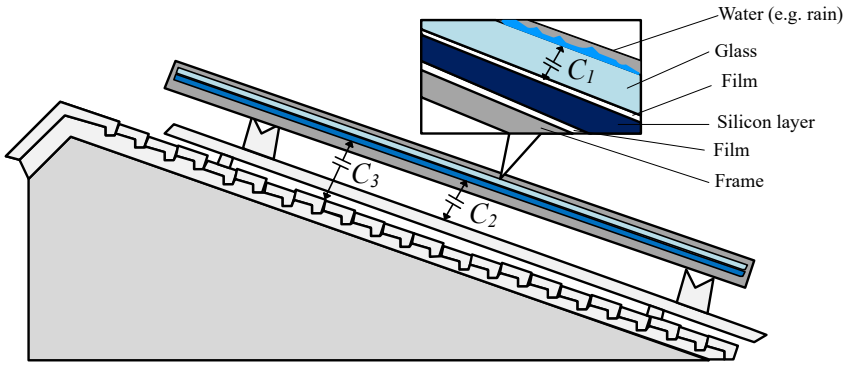

Fig. 1.12: PV module structure.

Considering the H-bridge topology shown in Fig. 1.13 which includes the most important stray elements such as capacitors and inductors. C_{pv} represents the stray capacitor formed between the PV module and the ground path, C_{1-2} represent the stray capacitances between the output terminals of the inverter and the ground point, Z_G is the impedance of the ground path, the stray capacitances of the EMI filter and ground point are defined as C_Y, also, L_{CM} and Z_{L1-L2} represent the EMI filter, phase and neutral impedances. It easy to observe that the common mode current (CMC) injected into the grid is only mitigated by the common mode impedances. Notice that, the CMC of the converter is equal to the LGC. Therefore, the CMC requires a path to return to the converter and this path is provided by the stray capacitances. In addition, it is well known that the LGC is a function of the common mode voltage (CMV) fluctuations, nevertheless, the LGC cannot be directly estimated from the CMV since it also depends on other factors such as systems stray elements and other voltage source [9], [16], [24].

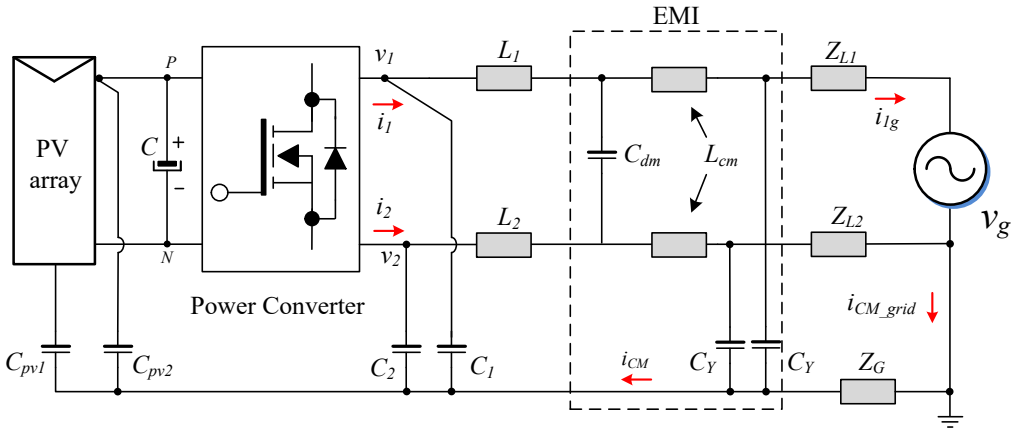

Fig. 1.13: TL systems with the most common stray elements.

Analyzing the H-bridge converter depicted in Fig. 1.13, the outputs v_1 and v_2 regarding to N point are considered, thus, the CMV is expressed as follows.

$$v_{cm} = \frac{v_{1N} + v_{2N}}{2}, \tag{1.1}$$

then, the differential mode voltage (DMV) is given by

$$v_{dm} = v_{1N} - v_{2N}. \tag{1.2}$$

From (1.1) and (1.2) the voltage at the output terminals of the converter can be represented regarding to N point, yields

$$v_{1N} = \frac{v_{dm}}{2} + v_{cm}, \tag{1.3}$$

$$v_{2N} = -\frac{v_{dm}}{2} + v_{cm}. \tag{1.4}$$

Now, taking into account the output currents of the inverter, the CMC is defined as

$$i_{cm} = i_1 + i_2, \tag{1.5}$$

the differential mode current (DMC) is given by

$$i_{dm} = \frac{i_1 - i_2}{2}, \tag{1.6}$$

expressing the inverter output currents in terms of common mode components yields

$$i_1 = i_{dm} + \frac{i_{cm}}{2}, \tag{1.7}$$

$$i_2 = -i_{dm} + \frac{i_{cm}}{2}. \tag{1.8}$$

Finally the injected current into the grid is i_1 which is the phase current of the inverter and it is given by

$$i_{1g} = i_{dm} + \frac{i_{cm}}{2}. \tag{1.9}$$

A path where the LGC can flow is not provided in isolated systems, in this case the CMC i_{cm} is close to zero, however, in a TL system the current i_{cm} is part of the injected current as it was described in (1.9). Therefore, the grid currents can be distorted by the contribution of i_{cm}. Performing a common mode model (CMM) of the H-bridge converter in Fig. 1.13 it turns out in the circuit depicted in Fig 1.14 [24]. It is worth noting that CMV is the sum of v_{cm} and v_{s1} where v_{s1} depends on v_{dm} and the L filter which has been split into two (L_1 and L_2) since in the trajectory of i_{cm} the position of the L filter is important due to i_{cm} flows both

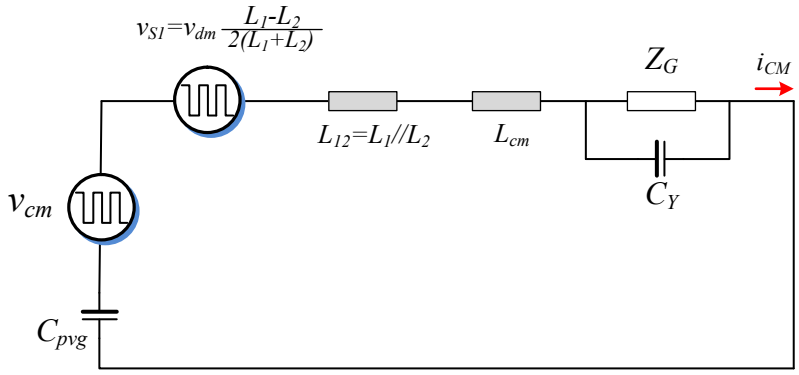

Fig. 1.14: Common mode model for H-bridge converter illustrated in Fig. 1.13.

through the phase and neutral conductor, that is, v_{s1} depends in the asymmetry of L_1 and L_2. In addition, as noted above, i_{cm} is limited by the common mode impedances and the impedance associated with the ground path, in this case the common impedances are fixed by the L filter L_{12}, EMI filter L_{cm} and Z_G, also the total stray capacitances of the PV module are defined as $C_{pvg} = C_{pv1}+C_{pv2}$. Thus, from the Fig. 1.14 a constant CMV is required in order to compensate the LGC. Normally, the varying CMV is associated with the switching of power semiconductors since the high frequency potential differences. One of the most common rule to limit the LGC is by the design of a specific sequence to switch the power semiconductors. Moreover, the inverter must guarantee the personal and equipment safety. For that, there are several standards that must be met in terms of LGC level and harmonic distortion, the latter since the LGC is directly related to the power quality certification. Several protection procedures and limitations of the LGC changes are established according to IEC 62109-2 and the kind of TL PV system. These limitations are listed in Table 1.1-1.2. As can be observed, any sudden change on residual current should trigger a break within a certain time in order to ensure the safety standards. For instance in Table. 1.1 a change of 30 mA represents a break time up to 300 ms. However, a sudden change of 150 mA for UL1741 requires a break time up to 40 ms. In other matters, in Table 1.2 the maximum break time is up to 300 ms for rated PV system lower than 30kVA, in addition, if the residual current is greatest than 300 mA the inverter must be alarmed. On the other hand, for PV system higher than 30kVA the residual current limit is 10mA/kVA.

Tab. 1.1: Residual current sudden change

Reference	**Residual current sudden change**	**Max. time to inverter disconnection from the mains**
IEC 62109-2: *Protection by residual current monitoring, Table 31*	30 mA	300 ms
CRD on UL 62109-1: *Reference to IEC62109-2 as before*	60 mA	150 ms
CRD on UL 1741: *Table 89.2*	150 mA	40 ms

Tab. 1.2: Excessive continuous residual current

Reference	**Power rating**	**Continuous Residual Limit [Max. disconnection time]**
IEC 62109-2 (Ed. 1.0): *4.8.3 Array residual current detection*	$\leq$30kVA AC power	300 mA [300 ms]
CRD on UL 62109-1: *Reference to IEC62109-2 (Ed. 1.0) as before*	>30kVA AC power	10 mA/kVA [300 ms]

2. STATE OF ART.

2.1 Transformerless photovoltaic systems

The main idea of implementing a TL PV system has been feasible due to the technological advance. Namely, removing the transformer from the PV system without side effects in terms of efficiency and integration to the grid. As a result of the modified structure, a simple, efficiency and inexpensive PV system is achieved. Nevertheless, as it was explained in the previous chapter, the TL inverter must be able to deal with the LGC issue. Consequently, many authors have addressed this trouble and design several solutions for that. Each strategy proposed in the literature is explained in this section with the purpose to provide a better outlook in terms of LGC solutions.

2.1.1 Techniques for reducing common mode currents

In general many solutions have been proposed to deal with LGC issue. Nevertheless, these solutions can be classified into the following global types:

1. Structure modification.
2. Modulation schemes.
3. Passive filters.

A description of the different forms of the leakage current mitigation in the TL PV system is shown below.

2.1.2 Structure modification

Structure modification has been well studied to address the leakage current issue which consists of adding semiconductors such as power switches and diodes in order to decouple the PV panel of the grid connection during freewheeling cycle and suppress the LGC level. Also this method can be used for clamping the output of the converter to neutral point and reduce the leakage current flow. Similar to latter strategy, in [17] the H5-converter freewheeling cycle is analyzed and then a new topology is proposed. H5-converter is depicted in Fig. 2.1(a) where the decoupling of the panel is achieved by S_1 during the freewheeling cycle. On the other hand, the topology proposed by [17] is shown in Fig. 2.1(b). It can be observed that this topology is formed of six power switches where the first and second one are being switched at high frequency in a complementary way. Moreover, S_2 connection allows to create a bidirectional clamping branch to ensure that the freewheeling path is clamped to the neutral point of C_{dc1} y C_{dc2}. Besides, power conduction losses are reduced since the output current is only flowing through three power switches during power processing. In addition, decoupling PV panel from grid is carried out by means of power switch connected at PV panel positive terminal.

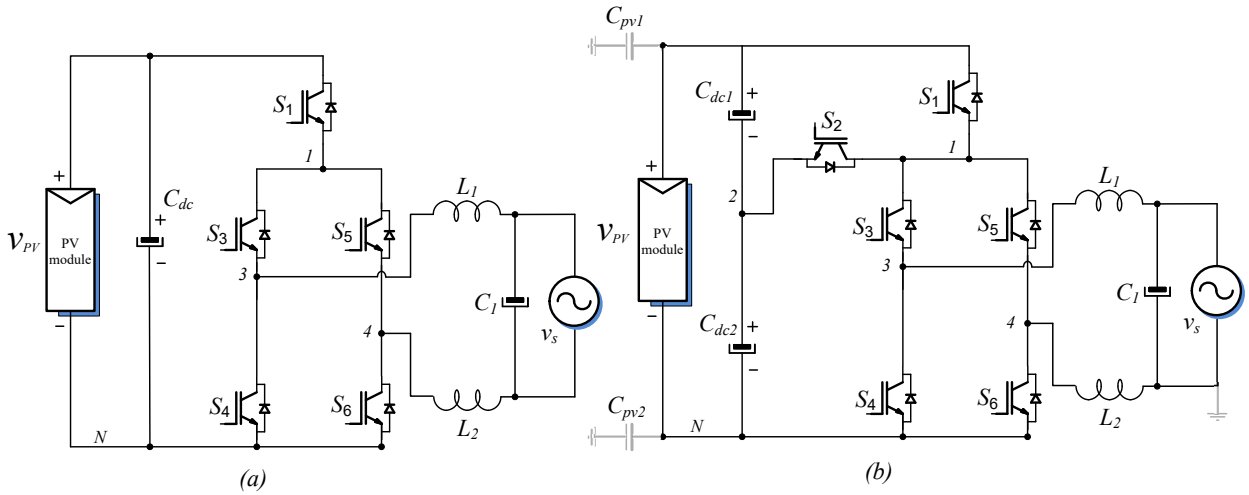

Fig. 2.1: (a) H5 topology y (b) Proposed topology in [17].

A resistor divider has been implemented to address the voltage unbalance issue in the DC capacitors, nevertheless, voltage balancing is not done effectively in the dead time of S_1 and S_2 and therefore, there is an increase in the leakage current because of the change in CMV.
Another alternative is analyzed in [18] where two asymmetric H-Bridge converters are performed. The first one is powered by a DC source, while the other is supplied through a floating

capacitor. This topology is depicted in Fig. 2.2. In general terms the output voltage is switching between two specific level voltages, and the limit of these levels is determined by the voltage of the DC source and the voltage of the capacitor.

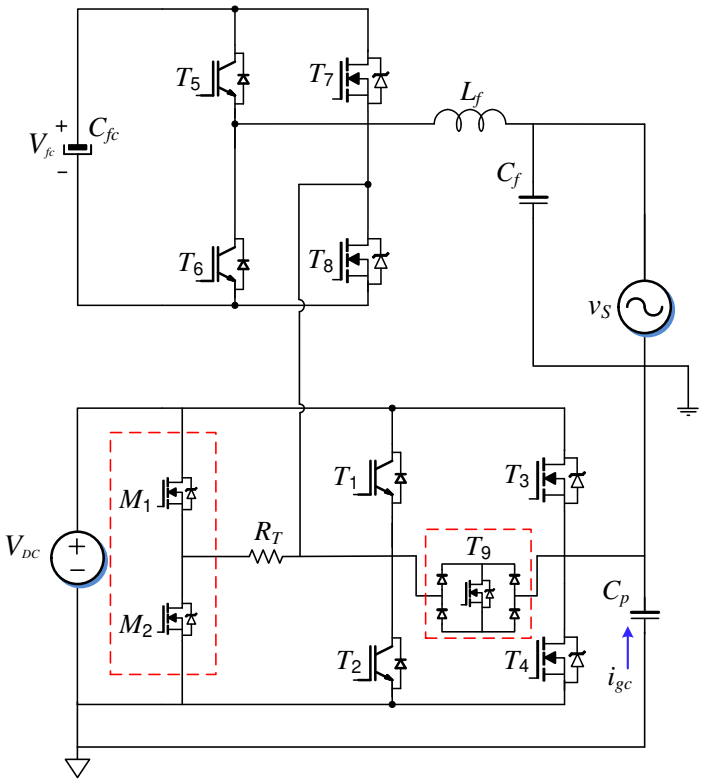

Fig. 2.2: Nine-level cascaded H-bridge proposed in [18].

Due to the capacitive coupling between the panel frame and ground, the CMC is inversely proportional to the switching frequency of the inverter branch connected to neutral, thus, in [18] a solution for the latter problem is that the aforementioned branch must switch at line frequency. In other matters, the topology has included an additional circuit to reduce the CMC and it is called transient circuit (TC) which is formed by two lower power semiconductors M_1 and M_2, one bi-directional switch T_9 and one resistance R_T as can be observed in the dot square of Fig. 2.2. TC circuit operation is based on turning on one of the MOSFET switches and also the bi-directional switch once the H-bridge converter is supplied with DC source producing 0 voltage at the output. In this case all switches of the lower H-bridge converter are in low state to keep a neutral potential floating by TC circuit operation. Therefore, a constant capacitor voltage is maintained. In all cases when the MOSFET switches commutation is swapped, that is, when slope of the zero crossing is positive or negative, stray capacitor voltage V_{C_P} is charged with a first order transient through R_T, limiting the increase in LGC.

Nevertheless, for a better performance of the TC circuit the grid voltage instantaneous angle is required. Besides, LGC could be less if a more accurate common mode filter design is implemented.

2.1.3 Modulation schemes

One of the most common technique for reducing LGCs in a TL PV systems is by modifying the switching pattern of the power semiconductor of the inverter topology, since in [24] has been demonstrated that CMC depends on CMV v_{CM}. Moreover, v_{CM} can be manipulated by a suitable modulation scheme design, in other words, with a specific switching sequence the variations of v_{CM} can be minimized and so that CMC is reduced. For instance, in [25] a modulation strategy is presented which is based on multicarrier pulse width modulation (MCPWM). The proposed modulation scheme to suppress CMC is a modified modulation technique of the phase opposition disposition (POD) PWM where only two carriers are required and it is referred by the authors as hybrid technique MCPWM (H-MCPWM). In addition, carriers phase are shifted $180°$ after each half cycle. Hybrid modulation technique operation can be analyzed in two modes as follows

- Mode 1: it has two commutation instants with v_{CM} equal to

$$v_{cm} = \frac{2V_{PV}}{4}, \tag{2.1}$$

$$v_{cm} = \frac{V_{PV}}{4}. \tag{2.2}$$

- Mode 2: it has three voltage levels for v_{CM}.

$$v_{cm} = \frac{2V_{PV}}{4}, \tag{2.3}$$

$$v_{cm} = \frac{V_{PV}}{4}, \tag{2.4}$$

$$v_{cm} = 0. \tag{2.5}$$

According to equations for Mode 1 and 2, the v_{CM} is limited into a range of values which produces less CMV variations, so that, the mitigation of LGC is achieved.
In other matters, a new modulation strategy is presented in [22]. This strategy consists on manipulating another classical MCPWM scheme, which is phase disposition (PD) PWM and as

a result a modified scheme MPDPWM for a five level CHB is obtained. The latter scheme is analyzed in two modes and they are given by

- Positive semi-cycle: all carrier signals are in phase and also the reference signal.
- Negative semi-cycle: all carrier signals stay in phase while the reference signal is shifted by one unit along the positive y-axis.

The switching strategy consists in properly selecting the operation states of the power switches with the purpose of keeping the CMV constant. In this case the number of carriers required is half of that required in PDPWM.
In [23] a novel modulation scheme is performed but now the authors analyzed all possible switching states for a five level CHB topology and a suitable pattern is chosen for minimizing CMV fluctuations, this modulation is called by the authors as Common-Mode Current Reduction Shifted Level Sinusoidal PWM (CMCR-SLSPWM). Nevertheless, CMV fluctuations occur during each change in the inverter output voltage level, hence the LGC waveform has spikes due to the CMV transient.

2.1.4 Filter solution

Implementing passive or active filters is another common method to reduce LGC, this method is based on adding passive or active elements (inductors, capacitors or power devices) to the filter connected between inverter output and the electrical grid. The authors in [19] propose an active filter, which is formed by a low power H-bridge converter and a common mode transformer. The magnetic element can be obtained by adding a third winding to the common mode inductors used at the main H-bridge converter output, this method is represented in Fig. 2.3. If an specific voltage is applied to the primary winding of the common mode transformer, the voltage of the secondary winding v_s can be used to cancel the CMV of the converter. The total CMV is given by,

$$v_{cmT} = \frac{v_{A10} + v_{B10}}{2} = v_{cm} - v_s, \tag{2.6}$$

According to (2.6) the voltage of the secondary winding must be equal to v_{cm} but without DC voltage component in order to keep a constant CMV. In addition, the gate signals for the H-bridge of the active filter can be obtained from the principal inverter. However, this method to switch the power devices of the active filter turns out in a delay during the rising and falling

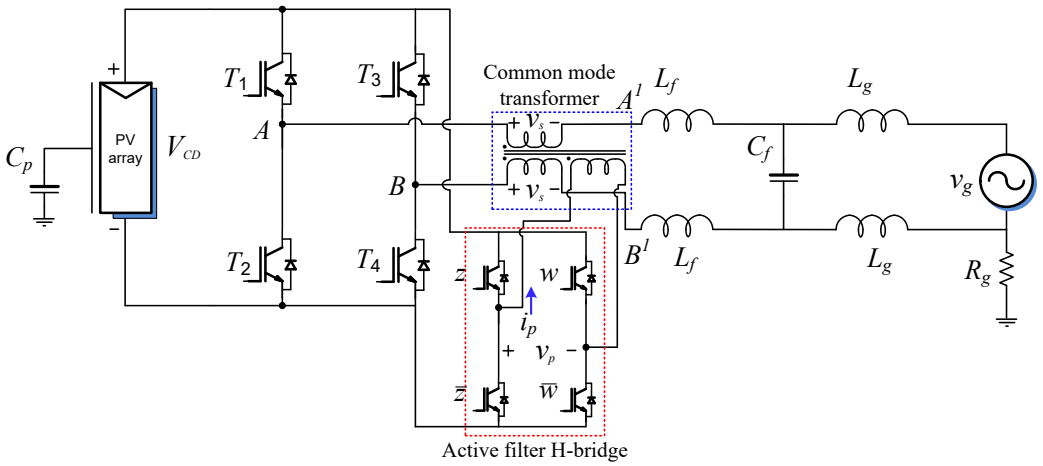

Fig. 2.3: Proposed inverter in [19] to reduce LGC.

edges of the switching signals and as a result a time difference is introduced between v_{cm} and v_s, which causes v_{cm} fluctuation with an interval equal to the dead time of the switching signals. This method turns out effective in terms of cost and size only if the compensation voltage and also the primary winding voltage v_p present a mean value equal to zero for each PWM period, since the mean value is no null, the magnetic core area or the turns number must be larger. Moreover, by adding the second converter the efficiency is affected.

In [20] two solutions to deal with LGC in CMI are presented. These solutions are also based on passive filtering. The first solution mainly applies to CMIs operated at high switching frequency, whereas the second method is used by CMIs operated at low frequency, as this method adds connections in the converter. The first topology which operates at high switching frequency is presented in Fig. 2.4, this topology consists on adding a DC-AC-side CM chokes and DC-side CM capacitors in each H-bridge module. This method allows to form a LC branch between DC-AC-side CM chokes and parasitic capacitances C_{pvn} in the equivalent common mode circuit. Therefore, with the purpose to attenuate LGC and obtain a good THD, the cutoff frequency of the LC filter must be lower than the switching frequency, also, this configuration must take into account filter design considerations which establish a limited value for the CM capacitors since the safety requirements [21]. Although, the cutoff frequency is lower than the switching frequency, the cutoff frequency cannot be selected too low, on the contrary, a large CM chokes are needed. Thus, the feasibility of this solution depends on the size and cost of the filter.

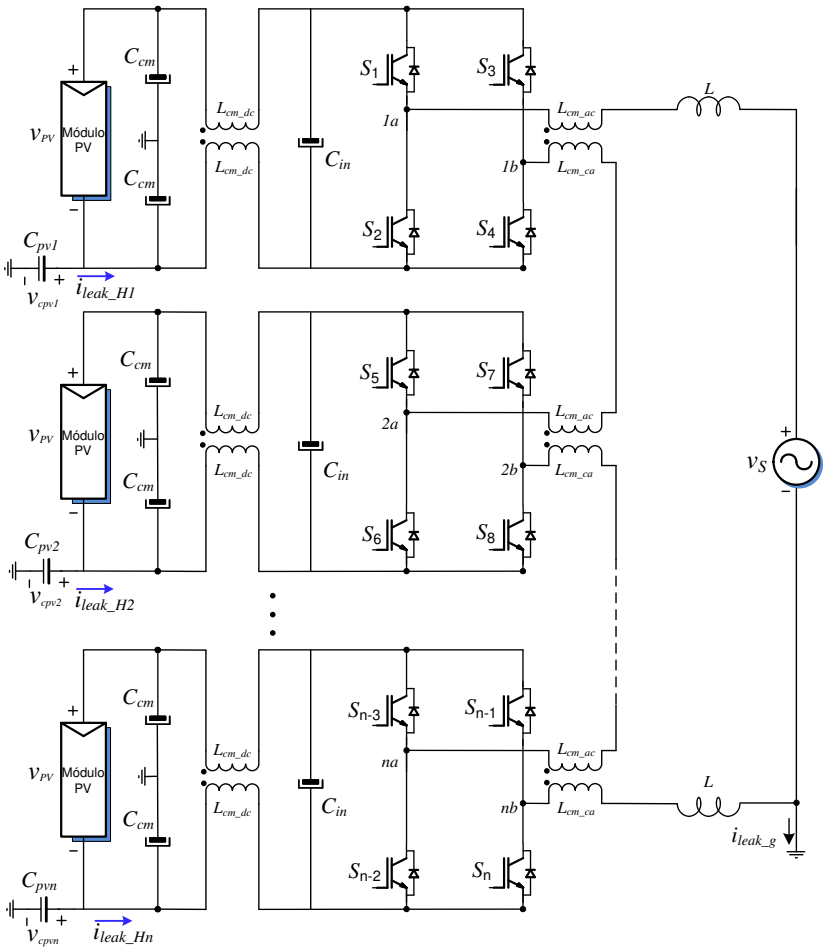

Fig. 2.4: Proposed solution in [20] for reducing LGC in high frequency CMI.

The second solution presented by the authors in [20] consists on including DC-AC-side CM chokes and capacitors. In this method there is a connection among the middle point of DC-side capacitors and the middle point of AC-side capacitors of each CHB inverter as it can be observed in Fig. 2.5. DC-AC-side capacitors are designed with a capacitance relatively larger than the parasitic capacitances , thus, the current of the parasitic capacitance can be attenuated if DC-AC capacitor currents is limited. The latter design allows a frequency not less than 1.5 kHz, besides, LGC RMS value increases as the parasitic capacitance value increases.

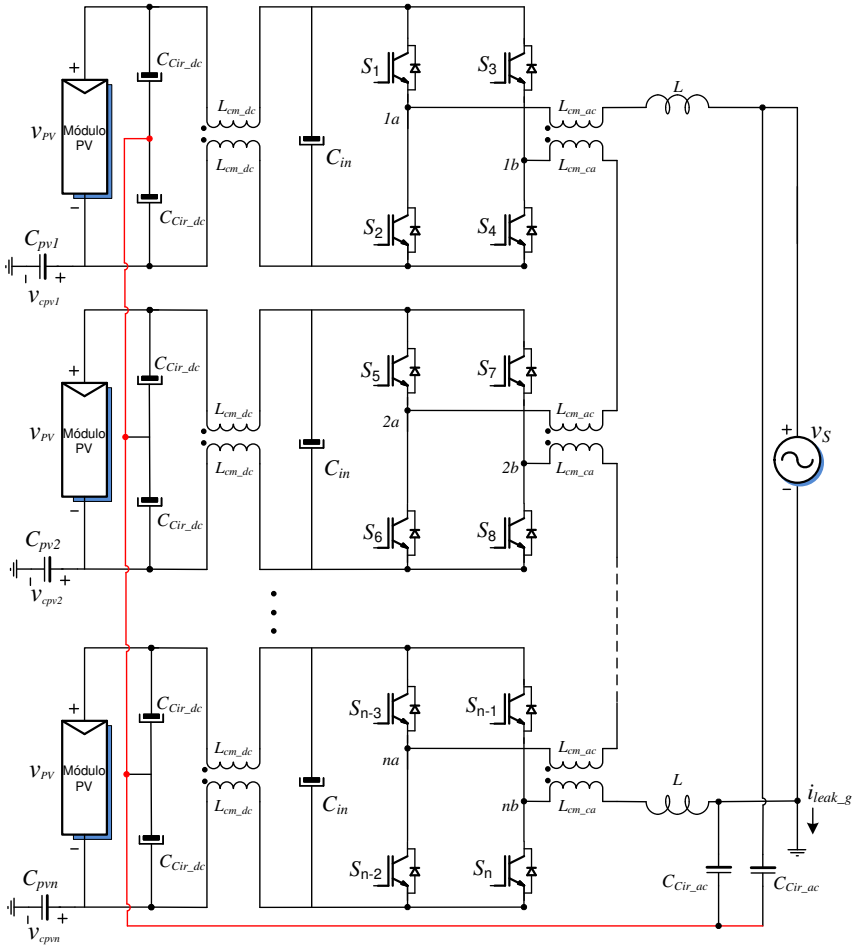

Fig. 2.5: Proposed filter in [20] for reducing LGC in low frequency CMI.

In order to alleviate LGC and the AC-side common mode electromagnetic interference noise a reconfigured passive filter connected at inverter output is performed in [26]. The proposed inverter is depicted in Fig. 2.6. For this topology extra semiconductors are not required, nevertheless, a CMC noise i_c circulates through the inverter, which is generated due to the CM propagation path formed by the proposed AC filter. i_c consists of a high and low frequency components and despite high frequency component is mostly applied onto CM inductor, the current i_c in the return path is low, although, a damping resistor is required in case the i_c increases, in other words, extra power losses are introduced.

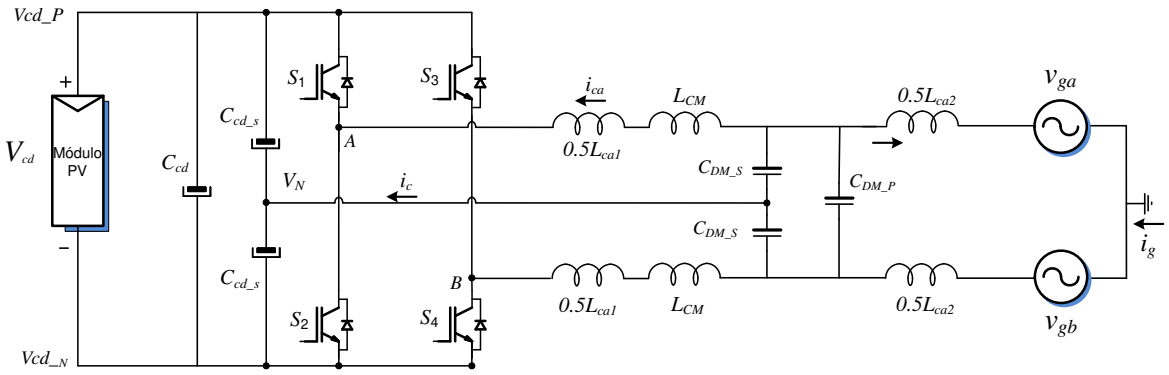

Fig. 2.6: Proposed structure by [26].

Another common issue in TL systems is the injection of DC DMC, this issue is mainly produced due to offset error in closed loop current measurement and analog-digital conversion. In [27] a circuit based on diodes, capacitors and resistors is proposed to prevent the DC DMC injection into the grid. The Fig. 2.7 shows the proposed circuit, as can be observed an extra electrolytic capacitor C_{CA} with a large capacitance is included in the basic H-bridge circuit, the purpose to include a large capacitance is to obtain a little reactance and as a result, a low AC voltage ripple is achieved. The inverter generates a DC voltage offset that is used to charge the electrolytic capacitor. Therefore, when DC voltage is higher than the AC ripple component, the electrolytic capacitance is not polarized and DC injection is prevented. Furthermore, multiples control loops are needed in order to generate a high quality current at the output and the DC compensation voltage of the electrolytic capacitor. Moreover, this technique must consider methods to protect the capacitor from reverse bias effect and transient conditions that cause overvoltages, for this reason, the topology include D_1, D_2, D_3 and D_4.

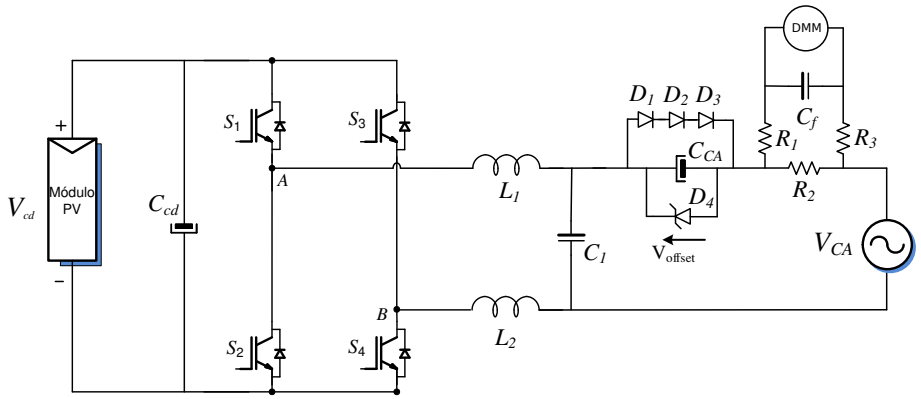

Fig. 2.7: Circuit proposed by [27].

3. PROPOSED SYSTEM ANALYSIS.

3.1 Topology description

In Fig. 3.1 the 5LCHB as a TL multilevel inverter with the proposed output filter solution is presented. This topology is formed by two CHB converters, which is able to synthesize five voltage levels. In addition, to deal with the LGC issues, a passive LC output filter is connected in the proposed configuration. This configuration consists of inductors symmetrically connected to each branch at the output of the inverter and capacitors connected from the end of each inductor to the DC-link. This connection avoid the injection of LGCs given that a low impedance path through the output filter is produced, as will be clear later in section 3.2.2. Thus, a symmetrical connection of the filter is necessary since each inverter branch contributes to CMV change. For Fig. 3.1, the proposed structure of the LC output filter L_1, L_2, L_3, L_4 and C_1, C_2, C_3, C_4 are used to represent the passive elements; v_{CDC1}, v_{CDC2}, v_{CDC3} and v_{CDC4} are the DC-link voltage; v_{C1}, v_{C2}, v_{C3}, v_{C4} represent the voltage trough the capacitors of the filter; i_{L1}, i_{L2}, i_{L3}, i_{L4} and i_{C1}, i_{C2}, i_{C3}, i_{C4} represent the current flowing through filter inductors (inverter side) and capacitors; i_1 and i_2 are the grid side currents. Regarding leakage current path, R_{GC} is the ground resistance and i_{GC} is the current flowing through R_{GC}. Besides, the stray capacitances formed between PV frame and N (neutral point of the grid) are represented as C_{P1}, C_{P2}, C_{P3}, C_{P4}. Notice that, two stray capacitances connected at the positive and negative point of the DC-link for each converter are considered. The magnitude of the capacitances also has an influence, whose values are in the rang of 60 nF/kW to 160 nF/kW [24]. On the other hand, it is worth mentioning that all voltages in this circuit are referred to the DC-link middle point (P_1 and P_2) for the differential and common mode analysis.

The solution to address the LGC issue in this paper is by implementing a passive filter in order to

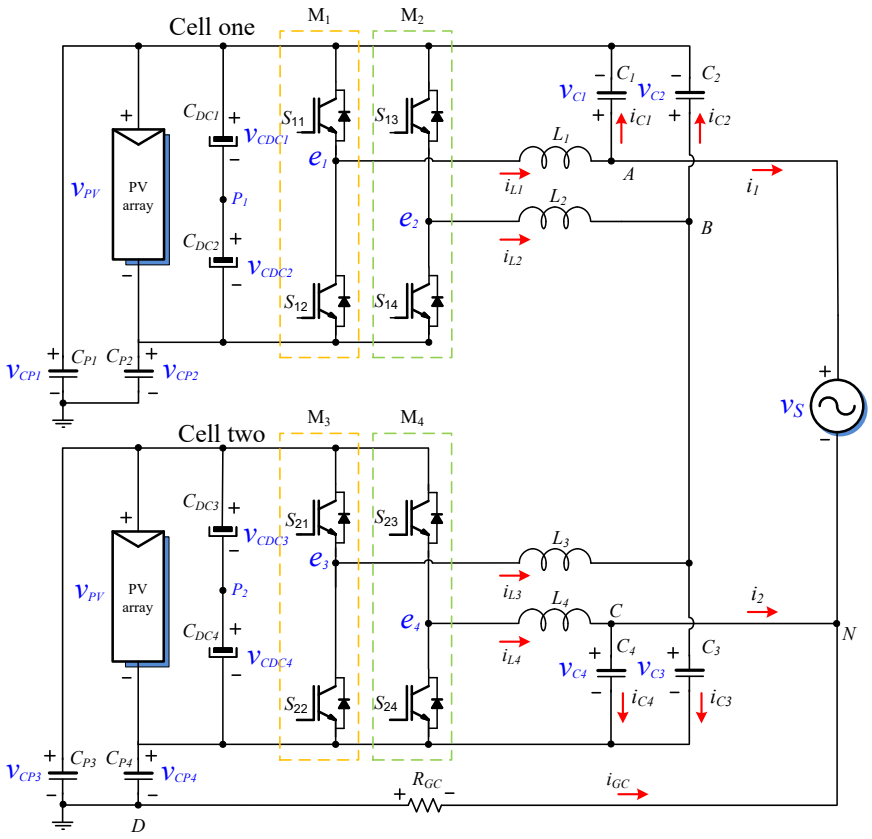

Fig. 3.1: Proposed topology.

create a new path where i_{GC} flows, this path is fixed through the connection of the filter capacitors. In other words, considering that the leakage current consists of high frequency current, if a new low impedance path is created, the LGC flow into the grid is prevented since the proposed filter provides this trajectory and forces the return high frequency leakage current through filter capacitors.

3.2 Common and differential mode model

The importance of the CMM is providing a better understanding of the LGC behavior. To develop the analysis of the CM and DM models, it is necessary to obtain a representation of the 5LCHB converter with LC filters tied to DC-link by applying Kirchhoff's voltage and current laws (KVL, KCL).

The outputs of the first cell are represented by the following equivalent circuits whose equations for Fig. 3.2 (a) and (b) are given by

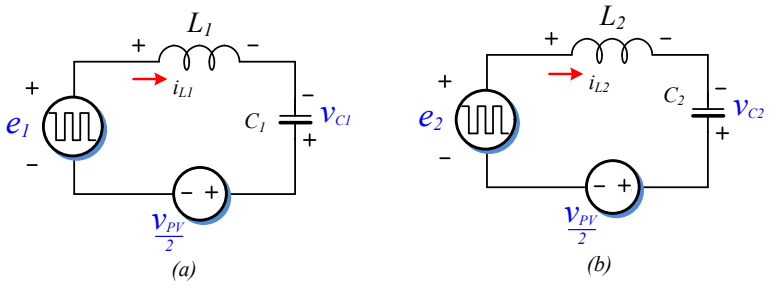

Fig. 3.2: Equivalent circuits to represent the outputs from the first HB converter.

$$L_1 \dot{i}_{L1} = -v_{C1} - \frac{v_{PV}}{2} + e_1, \tag{3.1}$$

$$L_2 \dot{i}_{L2} = -v_{C2} - \frac{v_{PV}}{2} + e_2. \tag{3.2}$$

To calculate the voltage across each output filter capacitors C_1 and C_2, the equivalent circuits shown in Fig. 3.3 are used.

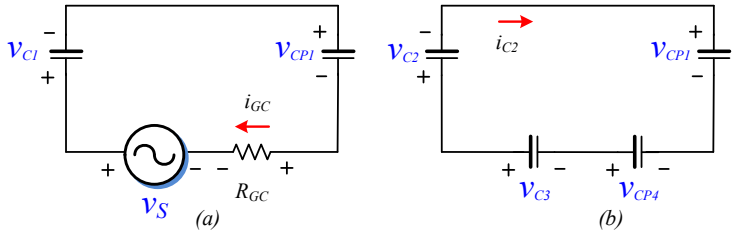

Fig. 3.3: Equivalent circuits for (a) C_1 and (b) C_2 voltage.

Applying KVL in the loop of each equivalent circuit shown in Fig. 3.3 (a) and (b). The equations (3.3) and (3.4) describe the voltage of C_1 and C_2.

$$\begin{aligned} v_{CP1} + R_{GC} i_{GC} - v_s + v_{C1} &= 0, \\ v_{C1} &= -v_{CP1} - R_{GC} i_{GC} + v_s, \end{aligned} \tag{3.3}$$

$$\begin{aligned} v_{CP1} - v_{CP4} - v_{C3} + v_{C2} &= 0, \\ v_{C2} - v_{C3} &= -v_{CP1} + v_{CP4}. \end{aligned} \tag{3.4}$$

Using a similar analysis for cell two, the equivalent circuits can be obtained which are represented in Fig.3.4.

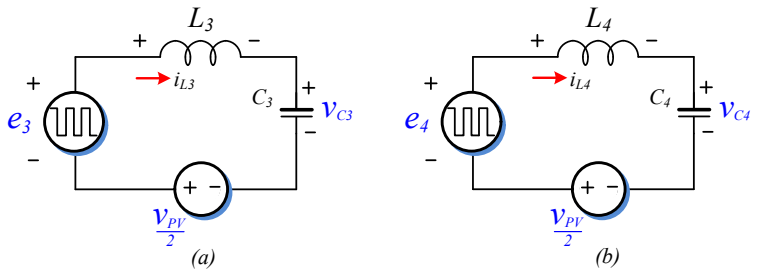

Fig. 3.4: Equivalent circuits to represent the outputs from the second HB converter.

According to Fig. 3.4, it is possible to calculate the voltage of the filter inductors L_3 and L_4 as seen below.

$$L_3 \dot{i}_{L3} = \frac{v_{PV}}{2} + e_3 - v_{C3}, \tag{3.5}$$

$$L_4 \dot{i}_{L4} = \frac{v_{PV}}{2} + e_4 - v_{C4}. \tag{3.6}$$

The expression for v_{C_4} is obtained considering the equivalent circuit depicted in Fig. 3.5.

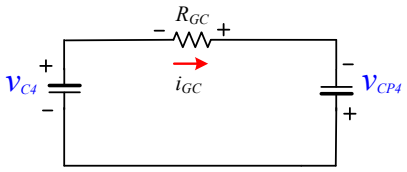

Fig. 3.5: Equivalent circuit for v_{C4}.

Thus, v_{C_4} is given by,

$$v_{C4} = -v_{CP4} - R_{GC} i_{GC} \tag{3.7}$$

The following set of equations are given by using KCL at A, B, C and D nodes of 5L-CHB topology observed in Fig. 3.1.

$$C_1 \dot{v}_{C1} = i_{L1} - i_1 \tag{3.8}$$

$$C_2 \dot{v}_{C2} + C_3 \dot{v}_{C3} = i_{L2} + i_{L3} \tag{3.9}$$

$$C_4 \dot{v}_{C4} = i_{L4} - i_2 \tag{3.10}$$

$$i_{GC} = C_{P1} \dot{v}_{CP1} + C_{P2} \dot{v}_{CP2} + C_{P3} \dot{v}_{CP3} + C_{P4} \dot{v}_{CP4} \tag{3.11}$$

Also, the circuit depicted in Fig. 3.1 keeps the following restriction

$$i_{GC} = -i_1 - i_2 \tag{3.12}$$

Regarding the CM and DM models the equations (3.3), (3.4), (3.7) and (3.12) must be considered. From now on it is assumed that $L_1 = L_2 = L_3 = L_4 = L$ and $C_1 = C_2 = C_3 = C_4 = C$ to obtain the CM and DM models.

3.2.1 Differential mode model

In order to obtain the differential mode model (3.8) and (3.10) are considered, which yields,

$$L\dot{\bar{i}}_{L1} = LC\ddot{v}_{C1} + L\dot{\bar{i}}_1, \tag{3.13}$$

$$L\dot{\bar{i}}_{L4} = LC\ddot{v}_{C4} + L\dot{\bar{i}}_2. \tag{3.14}$$

Substituting (3.13) and (3.14) in (3.1) and (3.6)

$$\begin{aligned} L\dot{\bar{i}}_1 + LC\ddot{v}_{C1} &= e_1 - v_{C1} - \frac{v_{PV}}{2}, \\ L\dot{\bar{i}}_1 &= e_1 - v_{C1} - \frac{v_{PV}}{2} - LC\ddot{v}_{C1}, \end{aligned} \tag{3.15}$$

$$\begin{aligned} LC\ddot{v}_{C4} + L\dot{\bar{i}}_2 &= e_4 - v_{C4} + \frac{v_{PV}}{2}, \\ L\dot{\bar{i}}_2 &= e_4 - v_{C4} + \frac{v_{PV}}{2} - LC\ddot{v}_{C4}. \end{aligned} \tag{3.16}$$

In addition, DMC injected into the grid is defined as,

$$i_{DMG} \triangleq \frac{i_1 - i_2}{2}. \tag{3.17}$$

Consequently, (3.13) and (3.14) are subtracted to obtain

$$L\dot{\bar{i}}_1 - L\dot{\bar{i}}_2 = \frac{(e_1 - v_{C1} - \frac{v_{PV}}{2} - LC\ddot{v}_{C1}) - (e_4 - v_{C4} + \frac{v_{PV}}{2} - LC\ddot{v}_{C4})}{2}, \tag{3.18}$$

reorganizing the last equation yields,

$$2L(\dot{\bar{i}}_1 - \dot{\bar{i}}_2) = (e_1 - e_4) - (v_{C1} - v_{C4}) - v_{PV} - LC(\ddot{v}_{C1} - \ddot{v}_{C4}). \tag{3.19}$$

Moreover, considering $e_{DM} = e_1 - e_4$, $v_s - v_{PV} = v_{C1} - v_{C4}$, the grid-side DMC can be described as,

$$\begin{aligned} 2L\dot{\bar{i}}_{DMG} &= e_{DM} - v_s + v_{PV} - v_{PV} - LC(\ddot{v}_s - \ddot{v_{PV}}), \\ 2L\dot{\bar{i}}_{DMG} &= e_{DM} - v_s - LC\ddot{v}_s, \end{aligned} \tag{3.20}$$

where e_{DM} is the DMV of the proposed converter. Additionally, a differential mode model (DMM) of inverter-side is obtained by subtracting (3.1) and (3.6) giving,

$$2L\dot{\bar{i}}_{LDM} = e_{DM} - v_s, \tag{3.21}$$

where $i_{LDM} = \frac{i_{L1}-i_{L4}}{2}$ is the inverter-side DMC. In addition, the DMV through C_1 and C_4 (v_{fDM}) can be obtained considering the expressions (3.8) and (3.10), thus v_{fDM} is given by,

$$C(\dot{v}_{C1} - \dot{v}_{C4}) = i_{L1} - i_{L4} - (i_1 - i_2). \tag{3.22}$$

Considering that $v_{fDM} = v_{C1} - v_{C4}$ the expression (3.22) can be rewritten as,

$$\frac{C}{2}\dot{v}_{fDM} = i_{LDM} - i_{DMG}. \tag{3.23}$$

Rearranging the DM expressions, the DMM of the proposed inverter with the second order filter is described by the following set of equations,

$$\begin{aligned} 2L\dot{i}_{LDM} &= e_{DM} - v_s, & (3.24)\\ \frac{C}{2}\dot{v}_{fDM} &= i_{LDM} - i_{DMG}. & (3.25) \end{aligned}$$

According to (3.24)-(3.25) the DMM circuit can be represented as it is shown in Fig. 3.6. Notice that the connection of the proposed passive filter turns out in a classic LC filter connection.

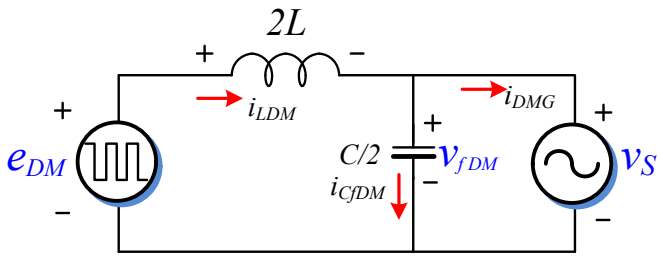

Fig. 3.6: Differential mode circuit of the proposed inverter.

3.2.2 Common mode model

The equations (3.8), (3.9) y (3.10) are used to represent the currents of the filter capacitors. Thus, adding (3.8) and (3.9) yields,

$$\begin{aligned} C(\dot{v}_{C1} + \dot{v}_{C2}) &= i_{L1} + i_{L2} - i_1 + i_{L3} - C\dot{v}_{C3}, \\ C(\dot{v}_{C1} + \dot{v}_{C2}) &= i_{CM1} + i_{L3} - i_1 - C\dot{v}_{C3}, & (3.26) \end{aligned}$$

where $i_{CM1} = i_{L1} + i_{L2}$. Based on (3.26) but considering cell two, the current through C_3 and C_4 is given by adding (3.9) and (3.10).

$$\begin{aligned} C(\dot{v}_{C3} + \dot{v}_{C4}) &= i_{L2} + i_{L3} + i_{L4} - i_2 - C\dot{v}_{C2}, \\ C(\dot{v}_{C3} + \dot{v}_{C4}) &= i_{CM2} + i_{L2} - i_2 - C\dot{v}_{C2}, & (3.27) \end{aligned}$$

where $i_{CM2} = i_{L3} + i_{L4}$. Therefore, in order to express the currents of the filter capacitors must be considered the current direction as defined in Fig. 3.1, then, (3.26) and (3.27) are added.

$$\begin{aligned} C(\dot{v}_{C1} + \dot{v}_{C2} + \dot{v}_{C3} + \dot{v}_{C4}) &= i_{CM1} + i_{CM2} + i_{L2} + i_{L3} - i_1 - i_2 - C(\dot{v}_{C3} + \dot{v}_{C2}), \\ C\dot{v}_{C\text{Filter}} &= i_{CMT} - i_1 - i_2 + i_{L2} + i_{L3} - C(\dot{v}_{C3} + \dot{v}_{C2}), \end{aligned}$$

but considering (3.9) and (3.12), the last equation can be rewritten as

$$\begin{aligned} C\dot{v}_{C\text{Filter}} &= i_{CMT} + i_{GC} - C(\dot{v}_{C3} + \dot{v}_{C2} - \dot{v}_{C2} - \dot{v}_{C3}), \\ 2C\dot{v}_{C\text{Filter}} &= i_{CMT} + i_{GC}, \end{aligned} \tag{3.28}$$

the expression (3.28) is based on the following definitions,

$$i_{CMT} = i_{CM1} + i_{CM2}, \tag{3.29}$$

$$v_{C\text{Filter}} = \frac{v_{C1} + v_{C2} + v_{C3} + v_{C4}}{2}, \tag{3.30}$$

where i_{CMT} is the total CMC and $v_{C\text{Filter}}$ represents the CMV of the filter capacitors. Therefore, (3.28) is a function of CMC and LGC.

Now, it can be obtained the total voltage of the filter inductors in terms of CMV, for that, is necessary to represent the sum of voltage across the cell one (L_1 and L_2) and cell two (L_3 and L_4). For cell one the voltage across the filter is given by adding (3.1) and (3.2).

$$L(\dot{\bar{i}}_{L1} + \dot{\bar{i}}_{L2}) = e_1 + e_2 - v_{C1} - v_{C2} - v_{PV}.$$

Considering $e_{CM1} = \frac{e_1+e_2}{2}$ in the latter equation, it yields

$$L\dot{\bar{i}}_{CM1} = 2e_{CM1} - (v_{C1} + v_{C2}) - v_{PV}. \tag{3.31}$$

On the other hand, for cell two the voltage across the filter is given by adding (3.5) and (3.6),

$$\begin{aligned} L(\dot{\bar{i}}_{L3} + \dot{\bar{i}}_{L4}) &= e_3 + e_4 - v_{C3} - v_{C4} + v_{PV}, \\ L\dot{\bar{i}}_{CM2} &= 2e_{CM2} - (v_{C3} + v_{C4}) + v_{PV}, \end{aligned} \tag{3.32}$$

where $e_{CM2} = \frac{e_3+e_4}{2}$. From here, the voltage dynamics of the filter inductors is represented by

$$\begin{aligned} L(\dot{\bar{i}}_{CM1} + \dot{\bar{i}}_{CM2}) &= 2(e_{CM1} + e_{CM2}) - v_{C1} - v_{C2} - v_{PV} - v_{C3} - v_{C4} + v_{PV}, \\ L\dot{\bar{i}}_{CMT} &= 2e_{CMT} - 2v_{C\text{Filter}}, \\ \frac{L}{2}\dot{\bar{i}}_{CMT} &= e_{CMT} - v_{C\text{Filter}}. \end{aligned} \tag{3.33}$$

Another restriction for CMM is deduced as follows. Simplifying (3.11) is proposed that $C_{P1} = C_{P2} = C_{PC1}$ and $C_{P3} = C_{P4} = C_{PC2}$, so that, can be rewritten as

$$2C_{PC1}\dot{v}_{CPC1} + 2C_{PC2}\dot{v}_{CPC2} = i_{GC}.$$

In addition, considering that all parasitic capacitances are equal, that is, $C_{PC1} = C_{PC2} = C_{PT}$, thus

$$\begin{aligned} 2C_{PT}(\dot{v}_{CPC1} + \dot{v}_{CPC2}) &= i_{GC}, \\ 2C_{PT}\dot{v}_{CPT} &= i_{GC}, \end{aligned} \tag{3.34}$$

where $v_{CPT} = v_{CPC1} + v_{CPC2}$. Furthermore, the proposed system keeps the restriction in (3.35) which is obtained by subtracting (3.3)-(3.7) and considering $v_{C\text{Filter}} = v_{C1} + v_{C4}$ and $v_{CPT} = v_{CP1} + v_{CP4}$.

$$2R_{GC}i_{GC} = v_s - v_{C\text{Filter}} - v_{CPT}. \tag{3.35}$$

From (3.28), (3.33), (3.34) and (3.35) the CMM can be drawn, and it is depicted in Fig. 3.7. As can be observed, with the inclusion of the specific connection of the proposed passive filter

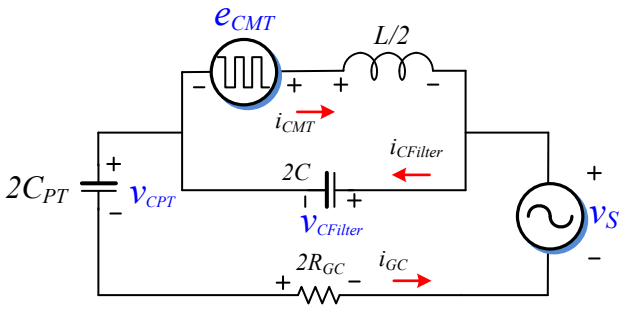

Fig. 3.7: Common mode model for 5LCHB with proposed filter.

a low impedance path is created where the high frequency components of the current grid can flow which allows minimizing the LGC up to a value close to zero.

3.3 Proposed filter analysis

As it was presented above the CMM of the proposed topology allows to describe the behavior of the LGC in the proposed solution and from the CMM circuit illustrated in Fig. 3.7 ensure that the proposed solution in this work is able to compensate de CMC in a CHB topology. On

the other hand, the DMM explains the behavior of topology tied to the grid. So that, it is important to address the DMM in this section since the filter design is based on the quality power standards, one of the most important standard is the THD, therefore, the filter design must be able to inject current into the grid with low harmonic distortion. Considering the DMM of the proposed topology, the filter analysis is performed as follows.

Taking into account the parasitic resistance R inherent in the filter inductors the set of expressions given by the differential mode model can be rewritten as follows,

$$\dot{i}_{LDM} = -\frac{R}{2L}i_{LDM} - \frac{1}{2L}v_{fDM} + \frac{1}{2L}e_{DM}, \tag{3.36}$$

$$\dot{v}_{fDM} = \frac{2}{C}i_{LDM} - \frac{2}{C}i_{DMG}. \tag{3.37}$$

Based on (3.36) and (3.37) the transfer function i_{LDM}/e_{DM} is obtained by using the Laplace transform. Therefore, $\frac{I_{LDM}}{E_{DM}}(s) = G_{DM}(s)$ is given by

$$G_{DM}(s) = \frac{\frac{1}{2L}s}{s^2 + \frac{R}{2L}s + \frac{1}{LC}}, \tag{3.38}$$

obtaining G_{DM} is a common practice for the frequency analysis, moreover, it allows choosing a suitable switching frequency to evade the harmful effects caused by the resonance peak, which is characteristic in a second order systems. According to second order systems, the frequency analysis can be performed by the characteristic polynomial $\Delta_{GDM(s)}$ which is given by,

$$\Delta_{GDM}(s) = s^2 + \frac{R}{2L}s + \frac{1}{LC},$$

where the natural frequency ω_n and the angular resonance frequency ω_r are defined as follows

$$\omega_n = \frac{1}{\sqrt{LC}}, \tag{3.39}$$

$$\omega_r = \omega_n\sqrt{1 - 2\left(\frac{R}{4\omega_n L}\right)^2}. \tag{3.40}$$

As previously mentioned, the proposed filter is able to mitigate the LGC since the proposed connection to the inverter, however, in grid-connected PV systems the output filter must be ensure the power injection with the desirable quality characteristics. In this case, the DMM equations turned out in a simple circuit with a typically LC filter connection as it was observed in Fig. 3.6, for this reason the design of the LC filter can be obtained from a classical LC filter design procedure. The design criteria procedure is based on [28], [29], [30], [31], [32] and several characteristics are considered, such as base values, based in the latter, the filter values

are chosen. These values are defined as follows

$$Z_b = \frac{V_{g,RMS}^2}{P_r}, \tag{3.41}$$

$$C_b = \frac{1}{\omega_g Z_b}, \tag{3.42}$$

$$L_b = \frac{Z_b}{\omega_g}, \tag{3.43}$$

where Z_b, C_b and L_b are referred as base impedance, base capacitance and base inductance respectively, and $\omega_g = 2\pi f_g$ is the angular grid frequency. Notice that, the base values are in function of the power rate (P_r) of the converter and grid RMS voltage ($V_{g,RMS}$). The considerations of the design criteria are enlisted bellow.

- Capacitor value is limited because of reactive power handled by the filter, which is less than 5% of C_b.
- The inductance is chosen in order to achieve a good performance according to the current ripple requirement, which is in the range of 15% to 40% of the peak value of the ouput current.
- The resonance frequency f_r must be between ten times of f_g and a half of f_{sw}.

Considering $V_{g,RMS} = 127$ V, $P_r = 1$ kW, the base values are the following,

$$Z_b = 16.129\ \Omega, \tag{3.44}$$

$$C_b = 164.46\ \mu\text{F}, \tag{3.45}$$

$$L_b = 42.783\ \text{mH}, \tag{3.46}$$

following the design criteria procedure, the capacitance value is defined as $C = 5\ \mu$F, which is less than 5% of C_b. Similarly, the inductance of L is chosen to accomplish the current ripple requirement at the inverter side, defining $L = 1$ mH, the maximum current ripple is given by the expression (3.47) used in [32]

$$\Delta_{i_L} = \frac{v_{PV}}{4Lf_s}, \tag{3.47}$$

$$\Delta_{i_L} = 2.75\ \text{A}. \tag{3.48}$$

Notice that the current ripple requirement is successfully reached. In other matters, defining $R = 2.58\ \Omega$, the resonance frequency can be determined and it yields,

$$f_r = \omega_r/2\pi, \tag{3.49}$$

$$= 2.25\ \text{kHz}.$$

The frequency analysis by numerical implementation is carried out by MATLAB software. Then, the Bode diagram is depicted in Fig. 3.8. Notice that, the resonance peak is according to f_r, whereas the harmonic attenuation is $20\ \mathrm{dB/dec}$. Regarding gain and phase margin, it can be observed that these parameters are infinite, which means that the dynamic of the filter is stable over the entire gain range.

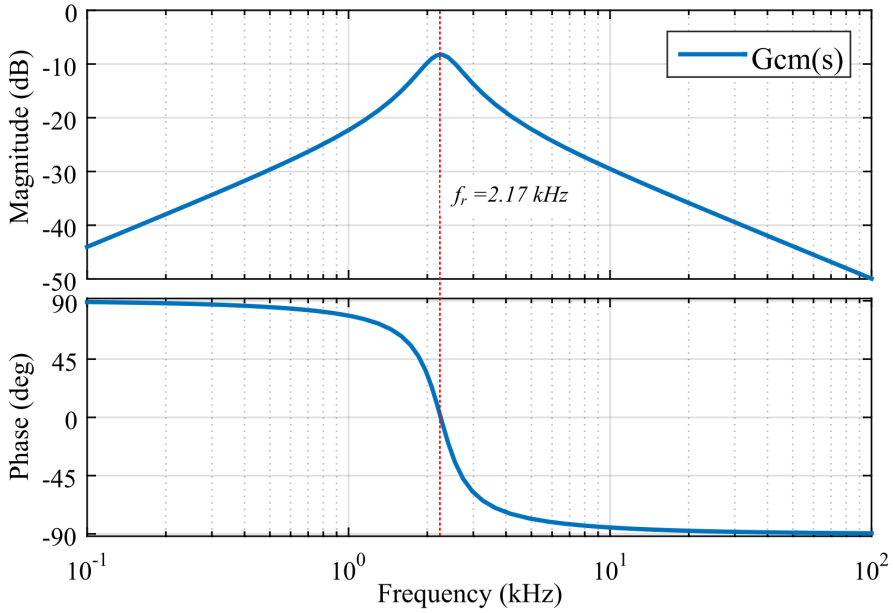

Fig. 3.8: Bode diagram for $G_{DM}(s)$.

The Fig. 3.9 shows the root locus plot of the $G_{DM}(s)$. The second order system has two complex-conjugate poles at $S_{1,2} = -\zeta\omega_n \pm \omega_n\sqrt{\zeta^2 - 1}$ and one zero at the origin. The poles are denoted by x whereas the zero are represented by o. The root locus shows the dynamic behavior of the filter when a parameter of the closed loop transfer function is changed, normally, this parameter is the proportional k. As a result of the root locus it can be seen that the dynamic of the proposed filter in closed loop is stable for any k value since the poles are in the left-side of the complex plane.

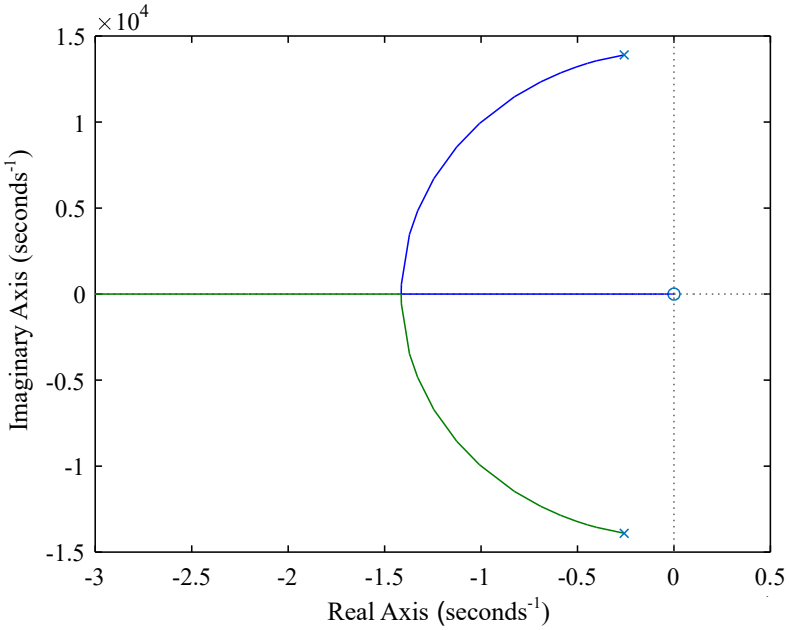

Fig. 3.9: Root locus plot for $G_{DM}(s)$.

4. NUMERICAL IMPLEMENTATION

4.1 Proposed PWM strategies

In order to validate the CMC behavior of the proposed system, a PWM technique is required. It should be noted that there are several contributions in this field in the literature which can be classified in: PWM, Pseudo-Modulation and closed loop control methods with implicit modulator [33]. Only the classical PWM modulation based on carriers are considered in this work, and these can be classified in: Level-shifted (LSPWM) and Phase-shifted PWM (PSPWM). These modulations are described below.
For the Level-shifted PWM:

- *In-phase disposition* (IPD). In this technique all the carrier signals are in phase.
- *Phase opposite disposition* (POD) where two carrier signals above the zero reference are in phase, whereas the remaining carrier signals are shifted 180° with respect to those above the zero reference.
- *Alternative phase opposite disposition* (APOD) where each carrier signal is shifted by 180°.

As it is mentioned above, the Phase-Shifted PWM method uses multiples phase-shifted carrier signals. In this type of modulation strategy, an appropriate phase shift angle is introduced between the triangular carrier waveforms in order to reduce the harmonic content of the output voltage. Due to the phase-shift of the carriers, a phase-shifted switching pattern is produced, which is used to generate a stepped waveform on the output voltage. In Fig. 4.1 the carrier

signals and the sinusoidal references for the PWM strategies involved are depicted. The gate signals for the proposed structure are obtained by comparing n carrier signals and one reference signal, which is a sinusoidal waveform at the grid frequency. The expression that represents the amount of the carrier signals n according to the number of voltage levels is given by

$$n = m - 1 \tag{4.1}$$

where m is the number of voltage levels at the inverter output [34],[35]. In addition, in the PSPWM method the phase-shift among the carrier signals is given by $\phi_{cr} = 360°/(m-1)$ or according to the number of cells by $180°/k$, where k is the number of cells, this method allows to cancel out all the harmonic content up to k^{th} carrier group [36]. The PSPWM and the level shifted methods are mainly used to modulate CHB converters due to the modularity of this topology, for that reason these techniques are chosen to be evaluated in this work. Moreover, most of the PWM techniques used to deal with the LGC issue are based on the level shifted methods because the computational resources are less than the other PWM techniques. On the other hand, the chosen PWM methods can be implemented in an easy way using a digital signal processor. In Table 4.1 the possible switching states for the 5LCHB to generate a five-level voltage waveform are summarized. Besides, in Table 4.2 the switching states used by each PWM technique regarding Table 4.1 are listed.

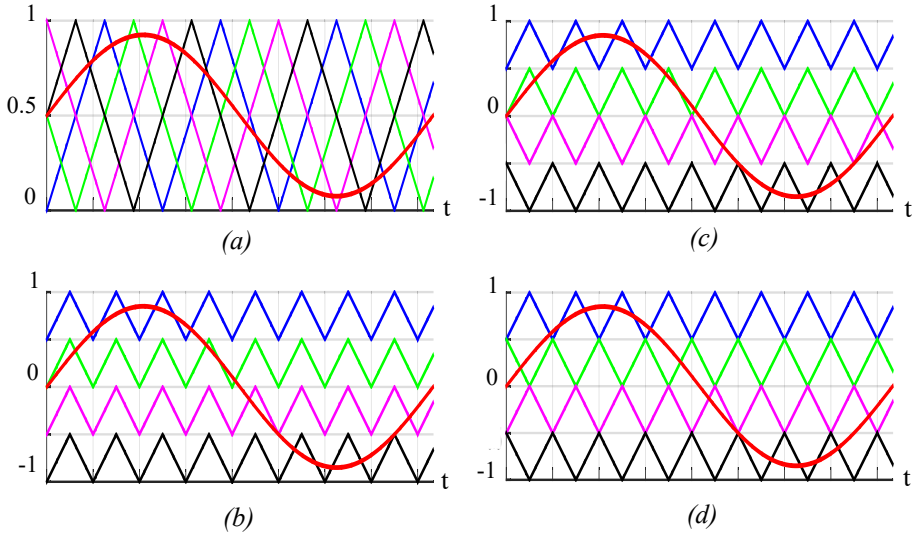

Fig. 4.1: Modulations strategies: (a) PSPWM, (b) IPD PWM, (c) POD PWM and (d) APOD PWM.

Tab. 4.1: Switching states for the 5LCHB inverter topology.

e_{14}	S_{11}	S_{12}	S_{13}	S_{14}	S_{21}	S_{22}	S_{23}	S_{24}	State
$2V_{PV}$	1	0	0	1	1	0	0	1	St1
V_{PV}	1	0	0	1	1	0	1	0	St2
	1	0	1	0	1	0	0	1	St3
	1	0	0	1	0	1	0	1	St4
	0	1	0	1	1	0	0	1	St5
0 V	1	0	1	0	1	0	1	0	St6
	0	1	0	1	0	1	0	1	St7
	1	0	0	1	0	1	1	0	St8
	0	1	1	0	1	0	0	1	St9
	0	1	0	1	1	0	1	0	St10
	1	0	1	0	0	1	0	1	St11
$-V_{PV}$	0	1	1	0	0	1	0	1	St12
	0	1	0	1	0	1	1	0	St13
	0	1	1	0	1	0	1	0	St14
	1	0	1	0	0	1	1	0	St15
$-2V_{PV}$	0	1	1	0	0	1	1	0	St16

Tab. 4.2: Switching states for each PWM technique.

e_{14}	**PSPWM**	**IPD**	**POD**	**APOD**
$2V_{PV}$	St1	St1	St1	St1
V_{PV}	St2	St5	St5	St5
	St3	–	–	–
	St4	–	–	–
	St5	–	–	–
0 V	St8	St9	St9	St9
	St9	–	–	–
	St10	–	–	–
	St11	–	–	–
$-V_{PV}$	St2	St12	St12	St12
	St3	–	–	–
	St4	–	–	–
	St5	–	–	–
$-2V_{PV}$	St16	St16	St16	St16

As it can be observed, the PSPWM method uses different switching combinations to generate five voltage levels in contrast to LSPWM that only uses one state per voltage level. An analysis regarding to the modulation index m_a is performed in order to evaluate the behavior of the THD in each PWM method without the proposed filter. So that, a five-level CHB with symmetric L filter is considered for this assess. Also, it is important to consider the frequency index m_f since the latter parameter plays an important role in the THD contribution. A common practice is selecting m_f as an odd integer number, then the harmonic reduction is achieved and also the sub-harmonics are avoided due to the odd symmetry of the signal. Considering f_m and f_c as the reference and carrier frequency, m_f is chosen as $m_f = 167$ and $f_m = 60$ Hz. That is, m_a and m_f can be calculated as follows [37],

$$m_{a,ps} = \frac{\hat{V}_m}{\hat{V}_c}, \tag{4.2}$$

$$m_{a,ls} = \frac{\hat{V}_m}{\hat{V}_c(m-1)}, \tag{4.3}$$

$$m_f = \frac{f_c}{f_m}, \tag{4.4}$$

where $\hat{V}_m$ and $\hat{V}_c$ are the peak amplitude of the reference and carrier signal respectively. In addition, $m_{a,ps}$ and $m_{a,ls}$ are the modulation index for the PSPWM and LSPWM method respectively. The THD of the output voltage ($THDe_{14}$) and grid current ($THDi_1$) versus m_a is depicted in Fig. 4.2.

Notice that, the $THDe_{14}$ is similar in all PWM methods, meanwhile in the $THDi_1$ results are better for the LSPWM methods because the LGC contribution in the PSPWM are higher which severely affects the THD of the grid current. It is worth mentioning that the results shown in Fig. 4.2 have been developed without LGC compensation. However, with a LGC compensation the $THDi_1$ of the PSPWM method is better than the LSPWM since the features in terms of effective frequency of the inverter ($f_{s,inv}$) is four times of f_{sw} instead of f_{sw} as in LSPWM methods.

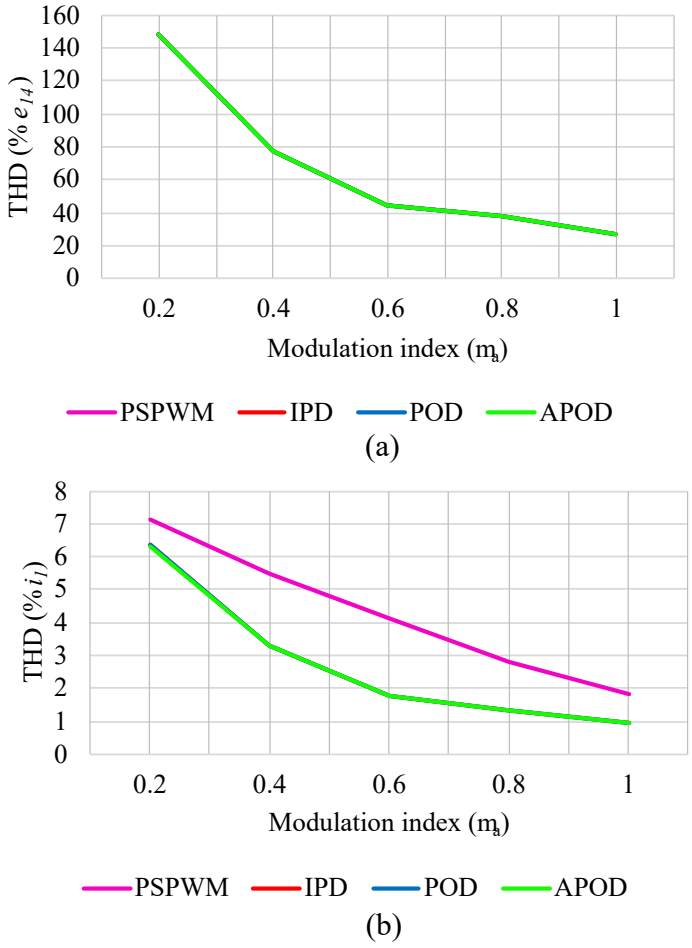

Fig. 4.2: THD values for (a) output voltage e_{14} and (b) grid current i_1 according to modulation index.

4.2 Comparative efficiency analysis

In order to obtain a power losses distribution analysis regarding conduction and switching losses for each power semiconductor of the PWM technique under study at the power rate the circuit of the Fig. 4.3 is considered. The circuit to perform the efficiency analysis is known as thermal module and it is implemented in the circuit simulation software with the key parameters of the physical IGBT module, in this case the SKM75GB12V is implemented in the experimental set-up, some of the parameters that were used to simulate the model are enlisted in the Table 4.3.

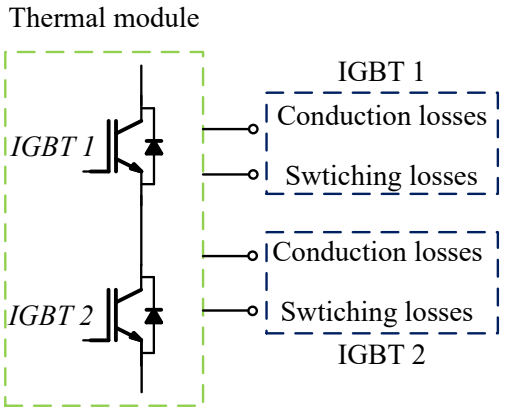

Fig. 4.3: Thermal module for IGBT module.

Tab. 4.3: Parameters for the SKM75GB12V thermal module.

Parameter	**Value**
$V_{ce,max}$ (V)	1200
$I_{c,max}$ (A)	114
$T_{j,max}$ (C)	175
$R_{th(j-c)}$ per IGBT (K/W)	0.38
$R_{th(c-s)}$ (K/W)	0.04
$R_{th(j-c)}$ per diode (K/W)	0.58

Also, several electrical characteristic for the IGBT and the diode are considered, this information was uploaded by means of graphics within the simulation software. These graphics are illustrated in Fig. 4.4-4.5, according to these electrical curves the simulation software can be estimate the conduction and switching power losses of the IGBT and the diode and provide four signal as can be seen in the Fig. 4.3, the first and second connection represents the conduction and switching losses for the upper IGBT, whereas the third and fourth connection represent the conduction and switching losses of the lower IGBT of the module. Is it worth mentioning that all information related to the IGBT module was obtained directly from the data sheet provided by the manufacturer.

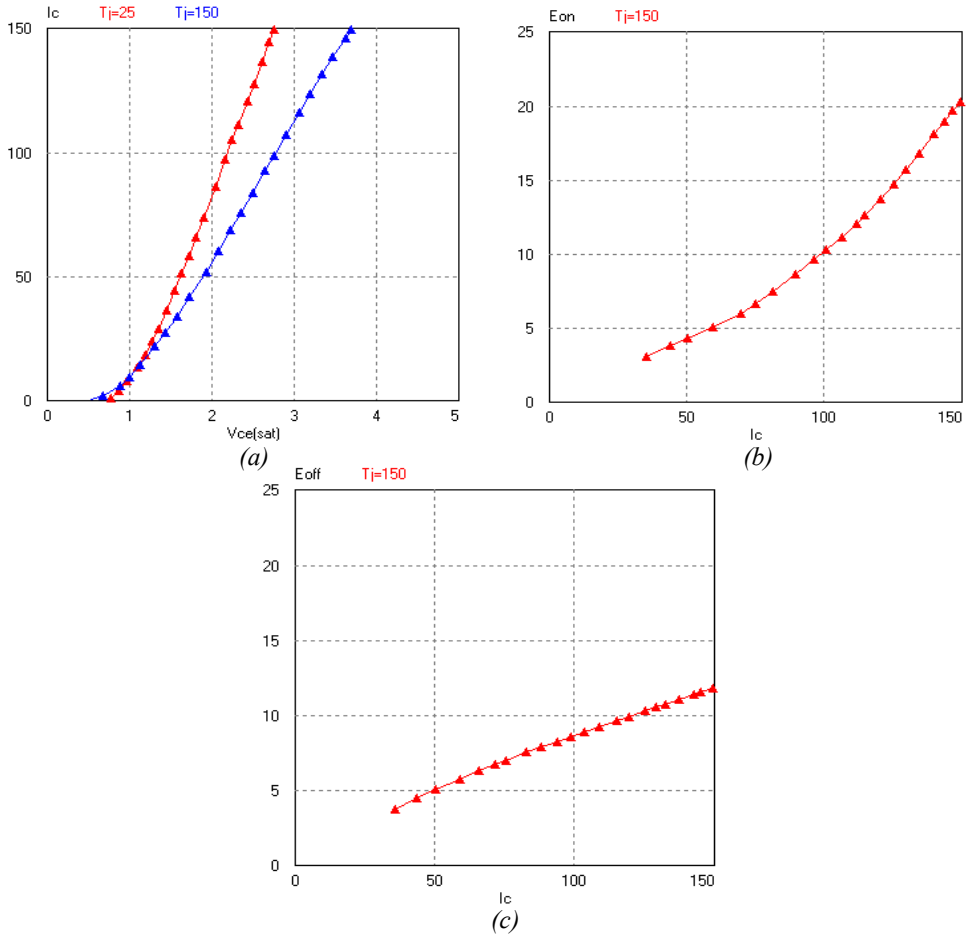

Fig. 4.4: Graphics for IGBT: (a) $V_{ce(sat)}$ vs I_c, (b) E_{on} vs I_c and (c) E_{off} vs I_c.

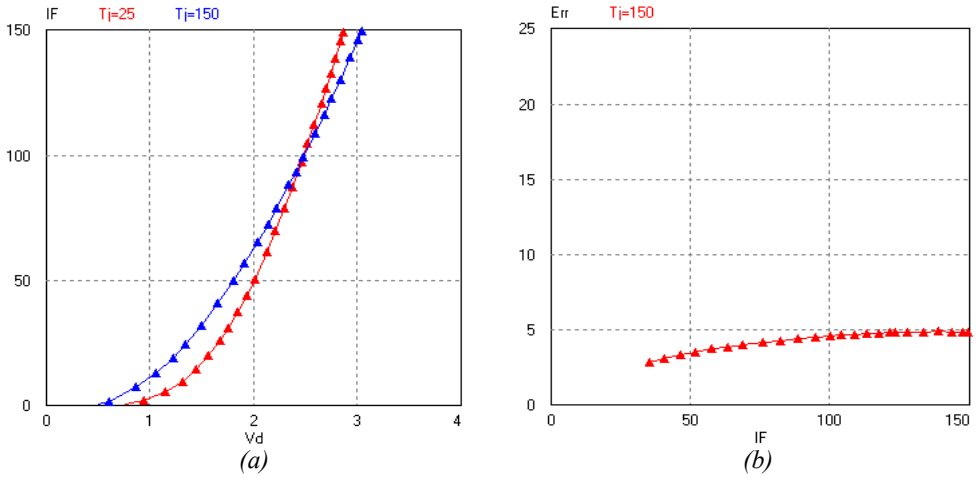

Fig. 4.5: Graphics for diode: (a) V_d vs IF and (b) E_{rr} vs IF.

As a result of the simulation of the proposed structure the Fig. 4.6 is obtained. With the purpose to simulate the 5LCHB inverter, four half-bridge IGBT modules ($M_1 = S_{11,12}$, $M_2 = S_{13,14}$, $M_3 = S_{21,22}$, $M_4 = S_{23,24}$) are considered as the Fig. 3.1 shows. It is quite clear that the power distribution losses are balanced in the PSPWM, on the contrary the LSPWM techniques have more conduction losses than switching losses due to the switching patterns. Comparing the results depicted in Fig. 4.6 it can be noticed that PSPWM has more power losses which affects the overall efficiency. A comparison between the PWM methods under study are summarized in Table 4.4.

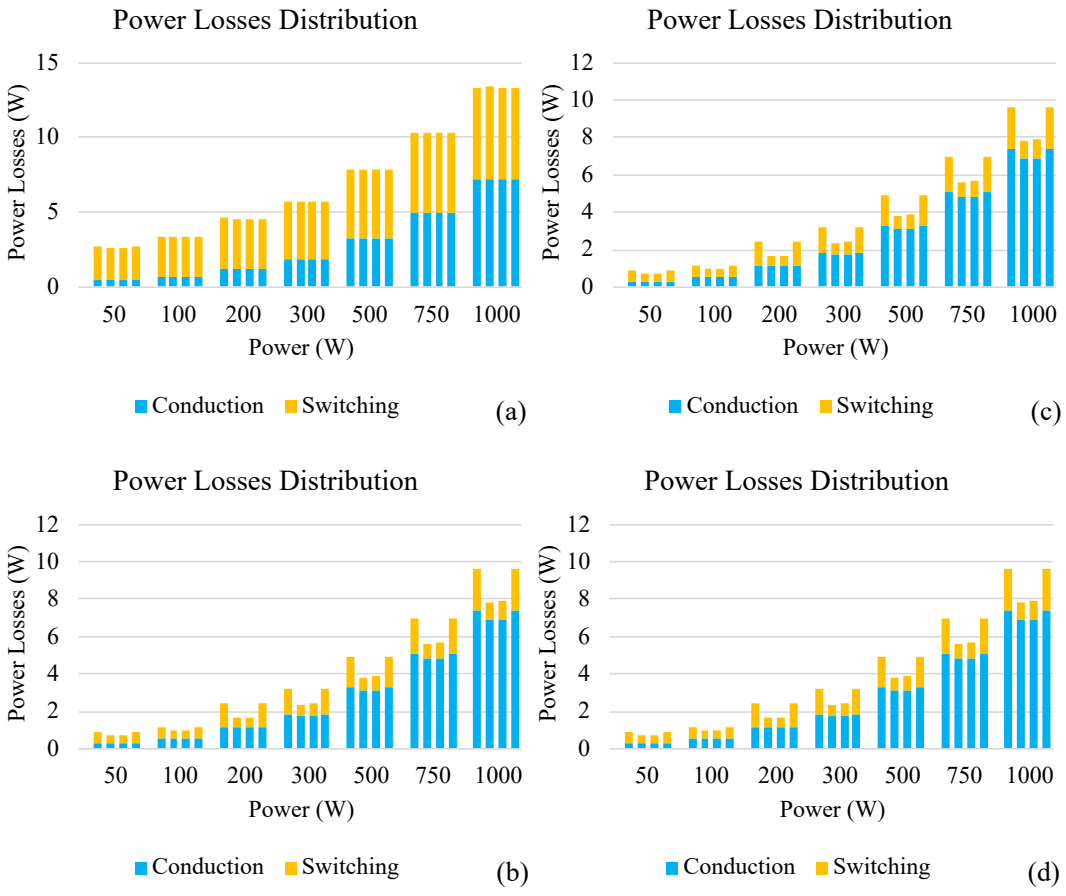

Fig. 4.6: Power losses distribution: (a) PSPWM, (b) IPD, (c) POD and (d) APOD (from left to right M1 to M4 are represented for each power rate).

Tab. 4.4: Comparison between the conventional PWM methods under study.

Parameter	**Phase Shifted Method (PSPWM)**	**Level Shifted Method (IPD, POD, APOD)**
Device switching frequency (f_{psw})	$f_{psw} = f_{cr}$	Different, an average is given by $f_{cr}/(m-1)$
Device conduction period	Same for all power switches	$Q_1 = Q_4, Q_2 = Q3$
Rotating of switching patterns	Not required	Required
Inverter frequency ($f_{s,inv}$)	$(m-1)f_{sw}$	equal to f_{sw}
Power losses distribution	same for all power semiconductors: conduction and switching losses are the same	$Q_1 = Q_4$, $Q_2 = Q3$, conduction losses are higher than the switching losses
Power losses per converter cell	same for all power cell	different for each power cell

Performing a comparative efficiency analysis and using the thermal Module of the IGBT it is possible to simulate the structure of the 5LCHB with power devices based on their data sheet, so that, a close real behavior of the power devices is obtained. Thus, the switching and conduction losses of the complete structure are calculated. The efficiency η of the proposed topology operating under each PWM method is calculated by (4.5) in a power range of $50\ \mathrm{W}$ to $1\ \mathrm{kW}$,

$$\eta = \frac{P_{in} - T_{losses}}{P_{in}}, \tag{4.5}$$

where P_{in} is the total power consumption on the DC side and T_{losses} represents the total power losses in each power switch of the inverter structure. Considering that the efficiency changes with respect to injected power level, the European efficiency (η_{EURO}) and the California Energy Commission efficiency (η_{CEC}) are calculated. The efficiency curves are depicted in Fig. 4.7, notice that, the curves for the level-shifted PWM schemes show higher efficiency values than the PSPWM strategy because the power devices are switching continuously along the grid period.

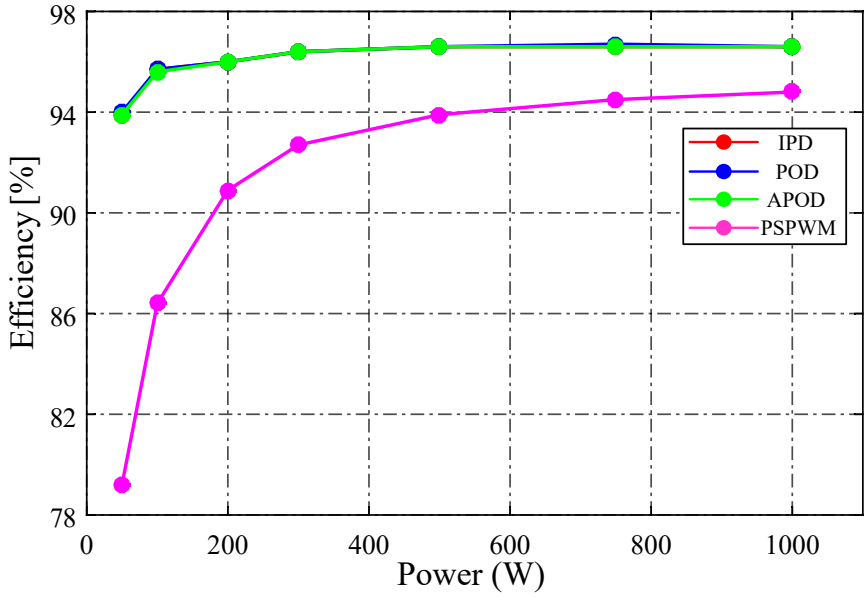

Fig. 4.7: Efficiency analysis for each modulation scheme.

4.3 Numerical results

Numerical implementation was performed in Power Sim ($\mathrm{Psim}^{\mathrm{TM}}$) software, and the thermal model of the IGBT SKM75GB12V is considered since this model allows to simulate the proposed converter closely to real implementation regarding power losses behavior. The numerical results for 5LCHB are presented in the following order: steady-state response without proposed filter, transient response, that is, connecting and disconnecting the proposed filter and steady-state with proposed filter. In Fig. 4.8 the inverter voltage, current grid and LGC are represented for PSPWM strategy. In this case, five-level voltage are synthesized at the inverter output, respect to LGC is around to 2 A peak. Notice that the waveform of the LGC for PSPWM is always changing and this behavior is due to the fact that the power semiconductors are switching during the whole grid period as consequence of the PWM sequence and produces a varying CMV.

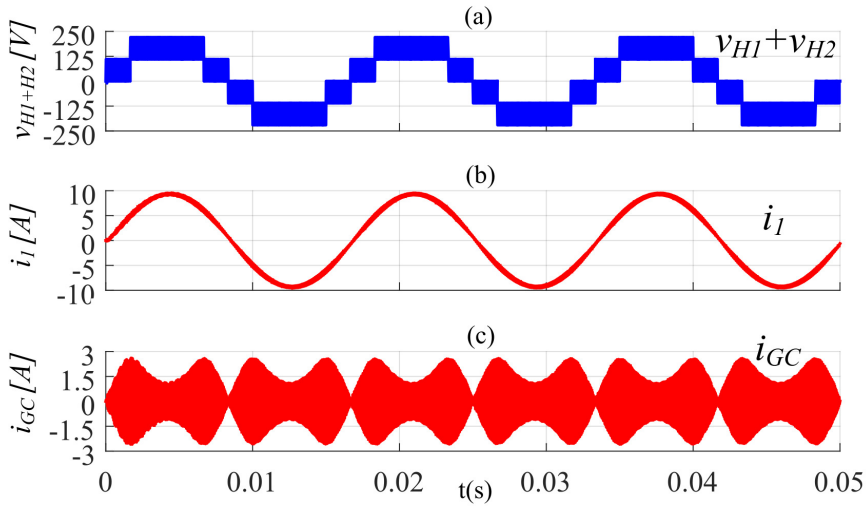

Fig. 4.8: PSPWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

The Fig. 4.9 shows the sum of each power cell output voltage in order to illustrated the five-level voltage waveform, also a sinusoidal grid current is obtained, however the LGC contribution is higher than the value establish by the safety standards, the peak current of the LGC is around to 1 A.

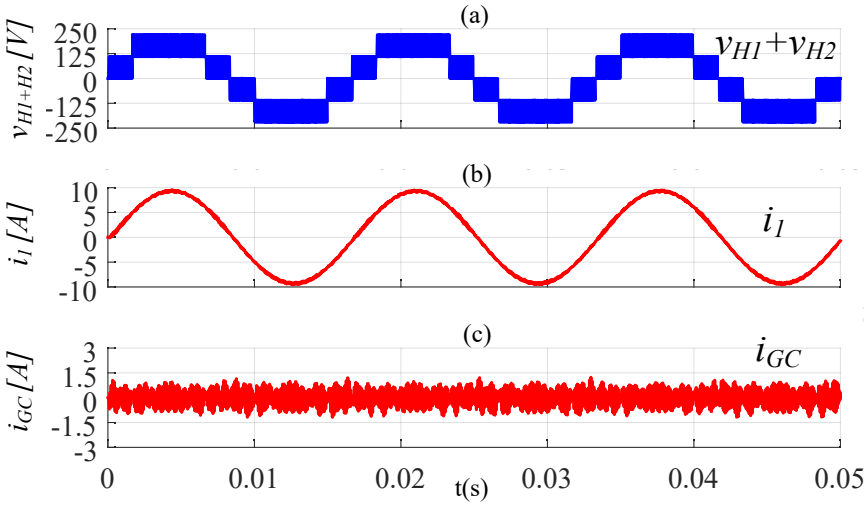

Fig. 4.9: IPD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

The simulations results for POD PWM technique are very similar to IPD PWM method as can be seen in the LGC waveform as well as the five-level voltage is obtained, these results are closely to the IPD PWM since the switching sequence are the same, however, the harmonic

contribution is different as it will show in the Chapter 5.

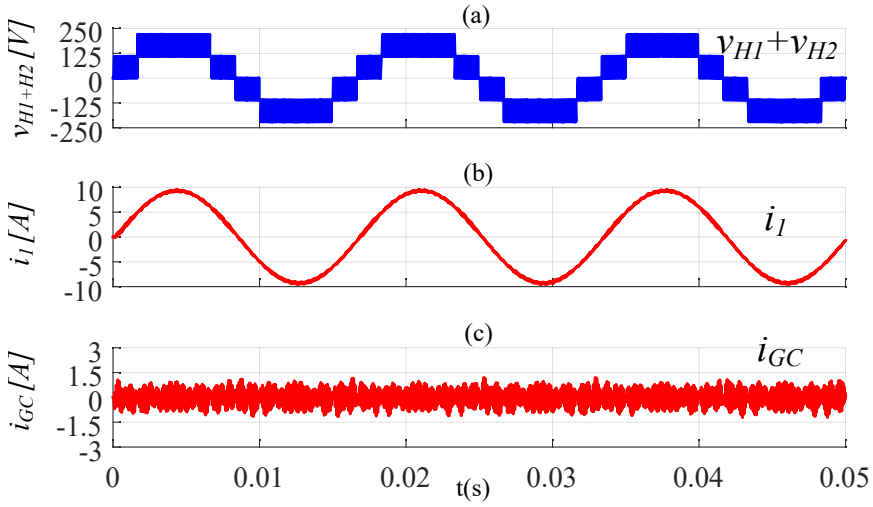

Fig. 4.10: POD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

In the Fig. 4.11 from top to bottom the output voltage, grid current and LGC waveform is depicted. The simulations results for APOD remain in the same magnitude as in the IPD and POD schemes, that is, 9 A_{peak} and 1 A_{peak} for i_1 and i_{GC} respectively. Although, the LGC magnitude is similar in all the LSPWM schemes, the harmonic distribution is not the same since the shifted angle of the carrier signals in each LSPWM method.

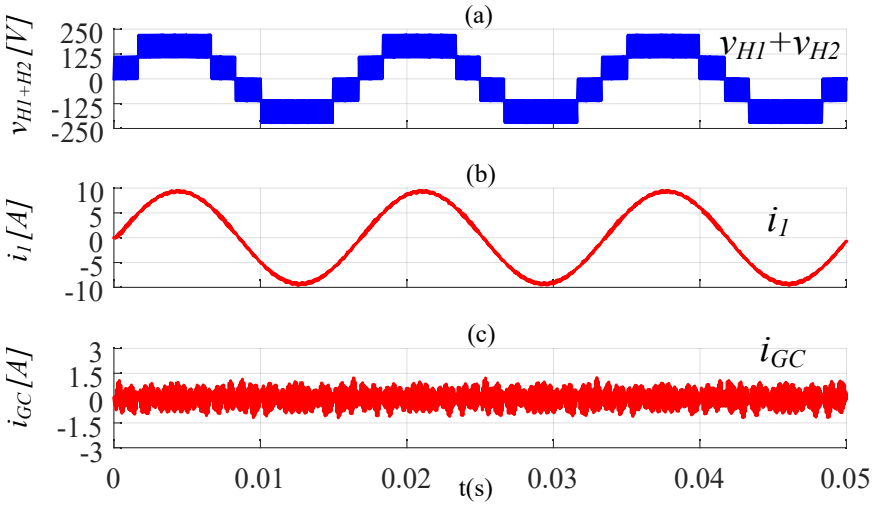

Fig. 4.11: APOD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

As a summary of the simulation results without the proposed filter, the four PWM strategies

are able to synthesized five-level voltage, it is easy to observe that the LGC waveform is different, although in the LSPWM is very similar in the three strategies. Comparing LGC magnitude, it is greatest in PSPWM than LSPWM methods, in the later method, that is, IPD, POD and APOD they have a maximum peak of LGC around to 1 A.

Analysing the transient response, the simulation results are showed in the range of 0.25 s to 0.35 s for grid currents (i_1, i_2) and i_{GC}, where the filter is connected at 0.3 s. The results for transient response of all PWM methods are illustrated in Fig. 4.12, 4.13, 4.14 and 4.15. Considering the PSPWM technique which has a high harmonic distortion in the grid currents, in specific i_2, it is easy to notice that the designed filter is able to filter the grid currents, which means that grid currents have less harmonic content when the filter is connected as shown in Fig. 4.12.

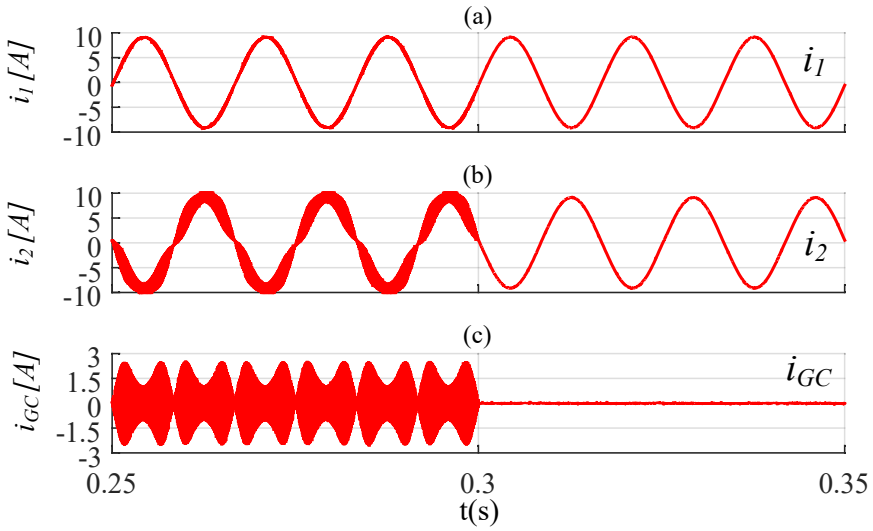

Fig. 4.12: PSPWM: (a) grid current i_1, (b) grid current i_2 and (c) LGC i_{GC}.

In Fig. 4.13 from top to bottom the grid currents i_1, i_2 and i_{GC} are depicted for IPD technique. It is quite clear that the high frequency components are filtered of the grid currents after the connection of the proposed filter, besides, the LGC magnitude decreases significantly to a level close to zero.

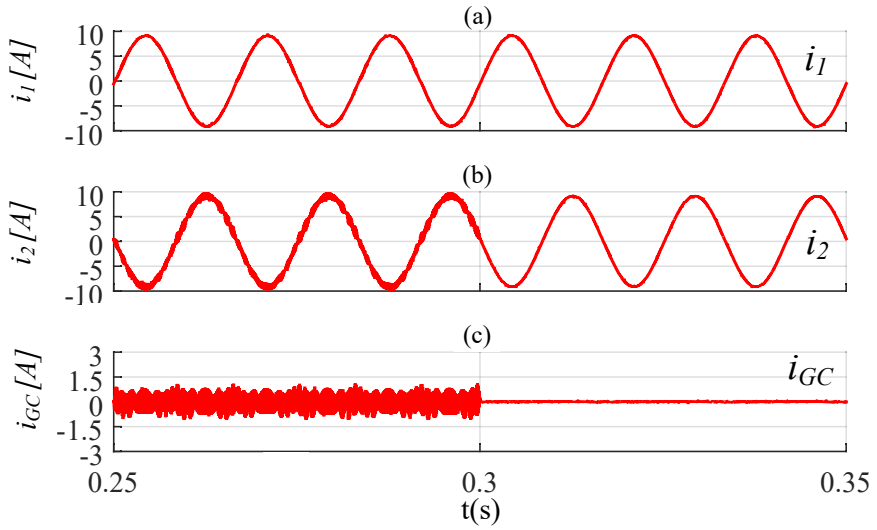

Fig. 4.13: IPD PWM: (a) grid current i_1, (b) grid current i_2 and (c) LGC i_{GC}.

For POD PWM method as can bee seen in Fig. 4.14 the simulations results show a similar behavior than the IPD method regarding to the grid currents and the LGC in the transient response. The LGC magnitud decrease from the 1 A peak to a value close to zero.

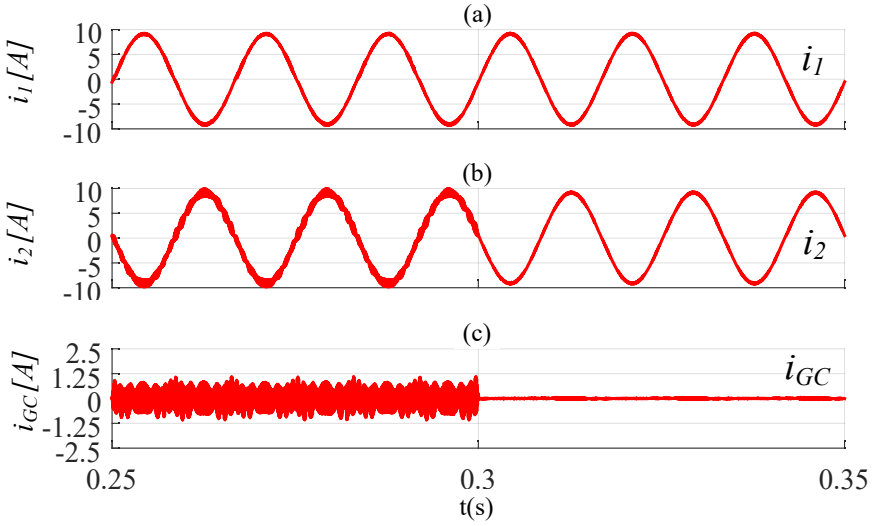

Fig. 4.14: POD PWM: (a) grid current i_1, (b) grid current i_2 and (c) LGC i_{GC}.

As can be observed in Fig. 4.15 from top to bottom the grid currents and LGC are illustrated for APOD PWM method, the filtering of the high frequency components from the grid currents and the mitigation of the LGC is achieved. As noted above, the simulation results for the LSPWM methods are very similar since the switching pattern is the same, on the other hand, the

difference between these methods is observed in the analysis of the harmonic spectrum shown in Chapter 5.

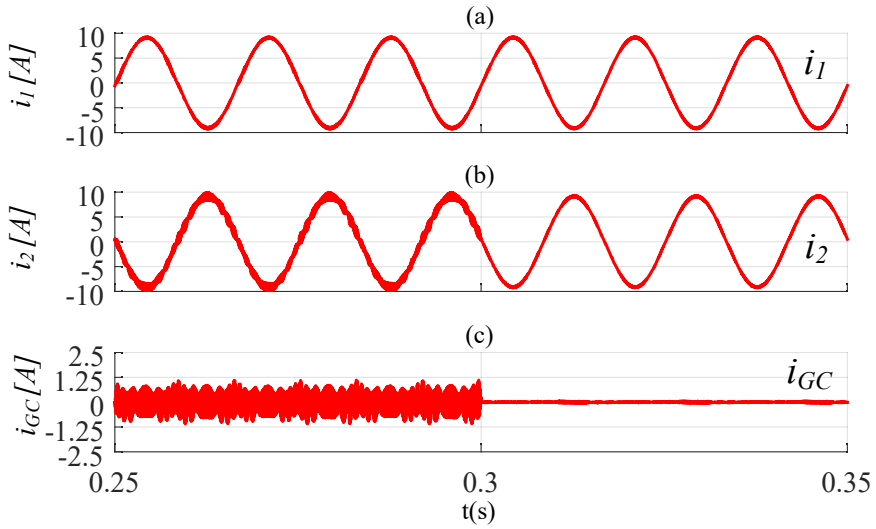

Fig. 4.15: APOD PWM: (a) grid current i_1, (b) grid current i_2 and (c) LGC i_{GC}.

The LGC compensation can be provided by plotting i_{CMT} and i_{GC} due to the filter connection forces most of the CMC to recirculate through the inverter instead of ground path. The Fig. 4.16-4.19 show the behavior of the CMC on the inverter side and LGC upon disconnection and connection of the proposed filter. It is expected that the CMC behaves different when the filter is connected. In case of IPD, POD and APOD methods the i_{CMT} magnitude is increased because of the proposed filter, nevertheless, for PSPWM technique is slightly modified. Therefore, an inconvenient has come up, that is, the high frequency components of the CMC are flowing by the switches. For instance, in LSPWM modulations the i_{CMT} has reached a peak value around to 2 A when the filter is on, whereas in PSPWM the peak value is kept at a similar range. However, this behavior in the CMC waveform represents a reduction in the lifespan of the semiconductors.

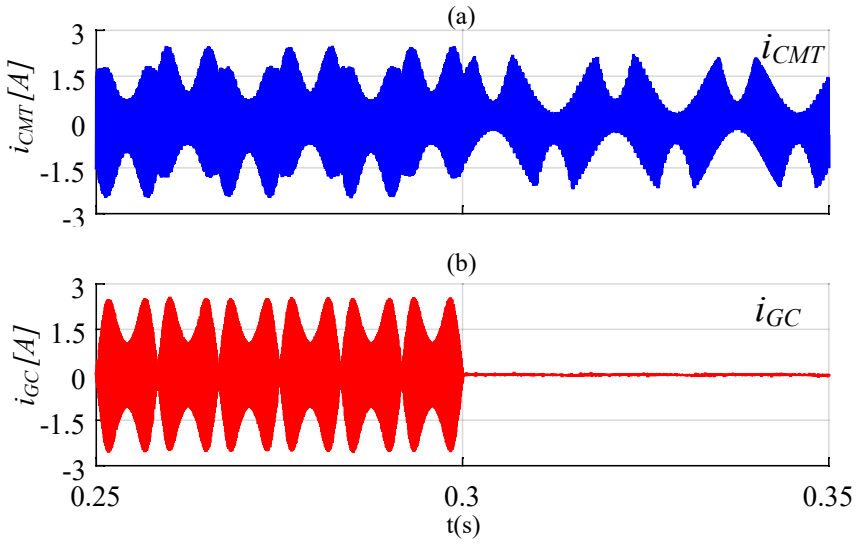

Fig. 4.16: PSPWM: (a) Total common mode current i_{CMT} and (b) LGC i_{GC}.

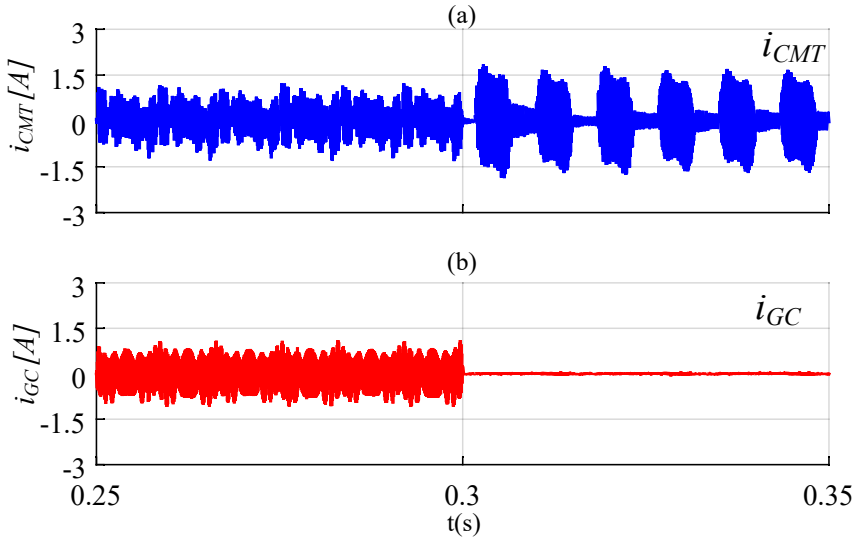

Fig. 4.17: IPD PWM: (a) Total common mode current i_{CMT} and (b) LGC i_{GC}.

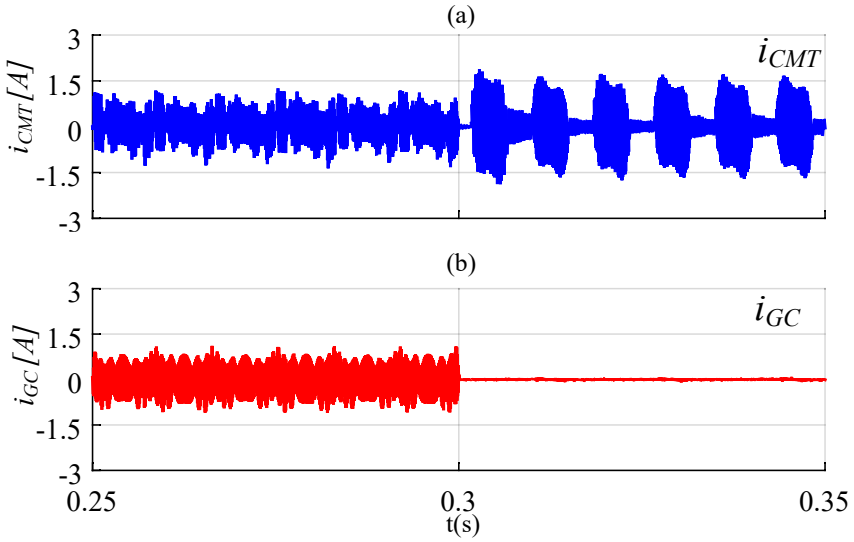

Fig. 4.18: POD PWM: (a) Total common mode current i_{CMT} and (b) LGC i_{GC}.

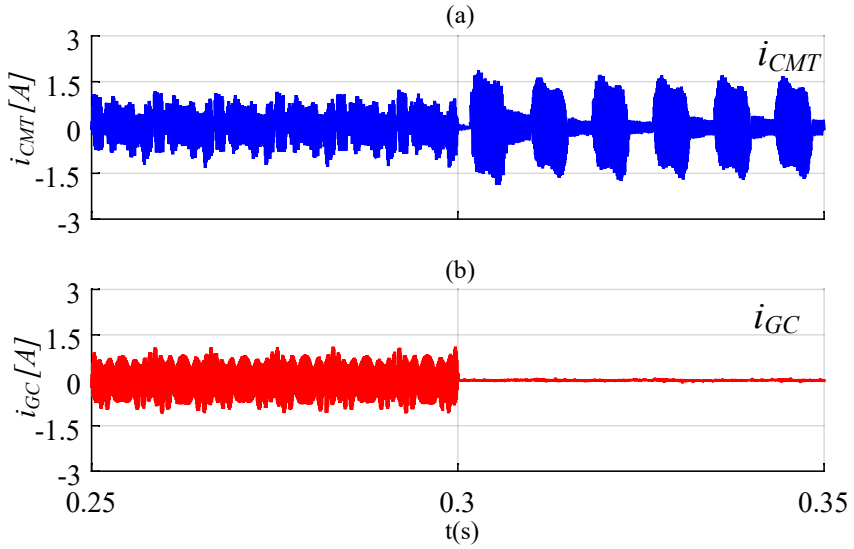

Fig. 4.19: APOD PWM: (a) Total common mode current i_{CMT} and (b) LGC i_{GC}.

The voltage through the stray capacitances are not easily accessible in a real implementation, moreover, by numerical simulation can be estimated the voltage waveform of these capacitances. In this work the voltage of v_{CP1} and v_{CP3} is only presented since the voltage of v_{CP2} and v_{CP4} is similar to the stray capacitances under study without DC component. Performing the transient analysis for the voltage of the stray capacitances, a time interval between 0.2 s to 0.4 s is considered. The importance to show the voltage v_{CP1} and v_{CP3} is to verify the dependency of the CMC regarding to the CMV. Notice that, in the Fig. 4.20-4.23 the CMV is changing along

the grid period for both capacitances. Moreover, the CMV contribution is higher in PSPWM than the LSPWM because the power devices are always switching which produces a high CMV contribution. Therefore, this type of PWM technique has a high peak value in the LGC as observed in Fig. 4.8.

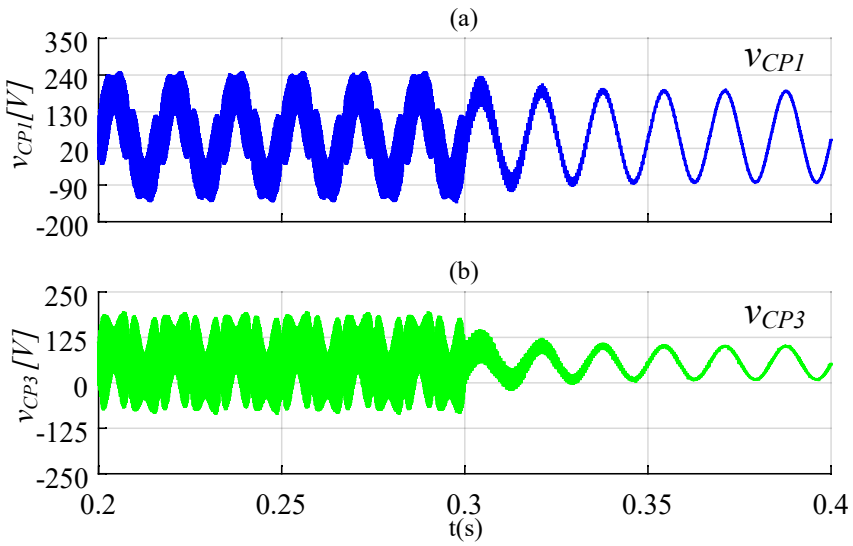

Fig. 4.20: PSPWM: (a) v_{CP1} and (b) v_{CP3}.

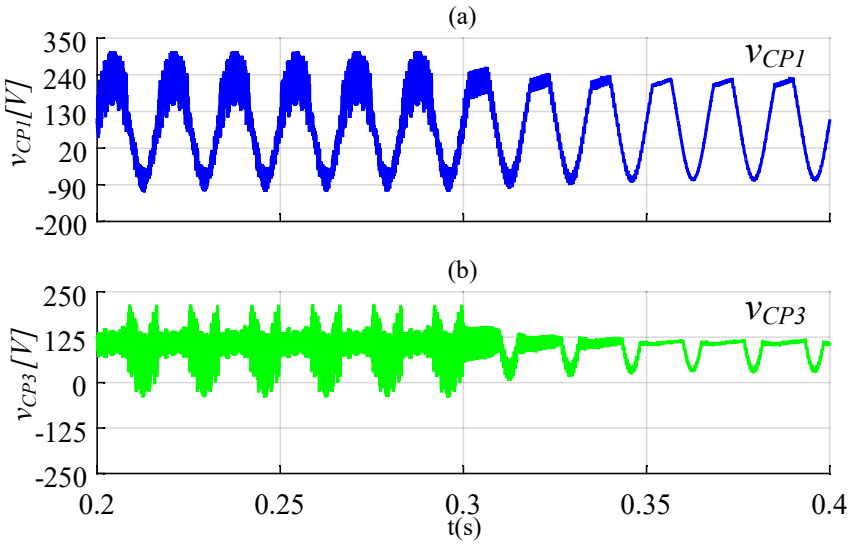

Fig. 4.21: IPD PWM: (a) v_{CP1} and (b) v_{CP3}.

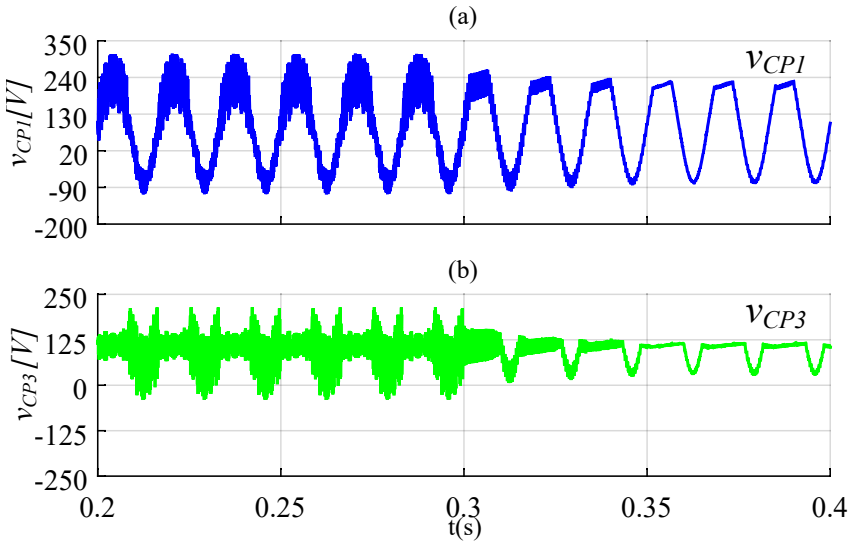

Fig. 4.22: POD PWM: (a) v_{CP1} and (b) v_{CP3}.

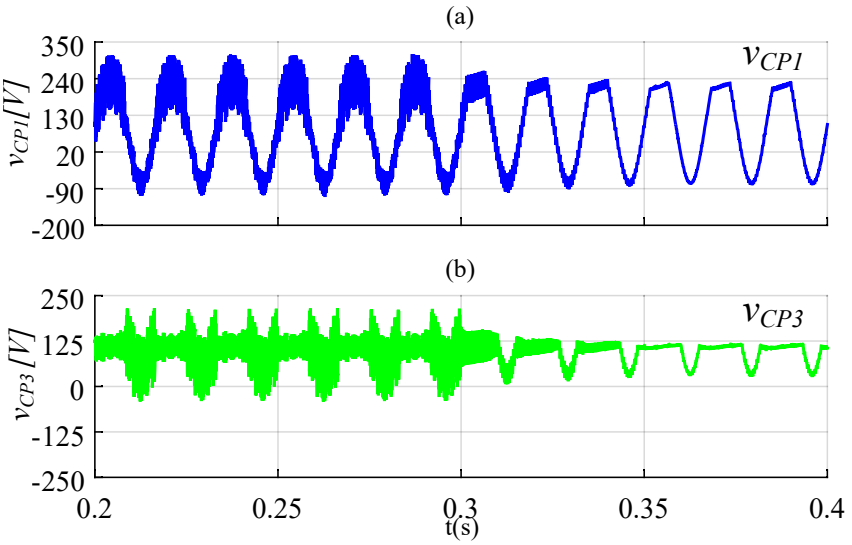

Fig. 4.23: APOD PWM: (a) v_{CP1} and (b) v_{CP3}.

Applying the proposed filter tied to DC-link the high frequency components in the CMV are alleviated for all cases under study. In case of PSWPM a waveform close to a pure sinusoidal is obtained. The CMV waveform for LSPWM methods seems a sinusoidal half cycle with a constant part. In fact the LGC magnitude is expected to be much lower for all PWM methods since the transitions in the CMV are mitigated. Then, the steady state response of the 5LCHB with the proposed filter is described bellow.

In the case of the steady state response the power rate is set to $1\ \mathrm{kW}$. The numerical results for

the modulations under study shown from top to bottom the five-level output voltage, the grid current i_1 which has a better quality regarding to THD and the LGC. In PSPWM method the LGC depicted in Fig. 4.24 has a peak value up to $50\ \mathrm{mA}$. Moreover, the LGC contribution is during the whole grid period and it was expected since the CMV waveform is a low frequency sine wave as can be observed in Fig. 4.20.

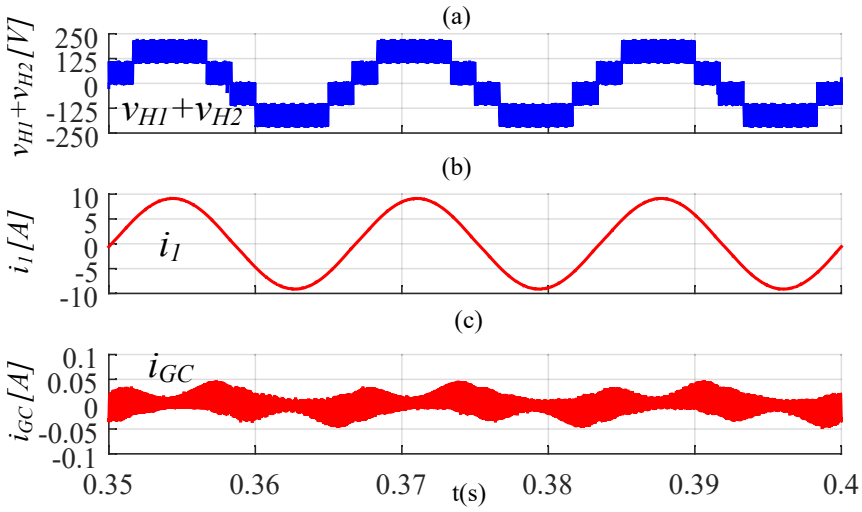

Fig. 4.24: PSPWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

For LSPWM modulations the simulation results are similar. Nevertheless, the LGC contribution is less than the PSPWM as can be seen in Fig. 4.25-4.27. Actually, the attenuation of the LGC reached in the positive semi cycle of the grid current is due to the constant part of the CMV. Consequently, the LGC magnitude increase during the negative semi cycle because of the fluctuation in the CMV. The RMS value for each PWM technique regarding LGC are calculate by means of a function of the simulation software and these measures are $16.02\ \mathrm{mA}$, $16.02\ \mathrm{mA}$, $16.01\ \mathrm{mA}$ and $16.77\ \mathrm{mA}$ for IPD, POD, APOD and PSPWM respectively.

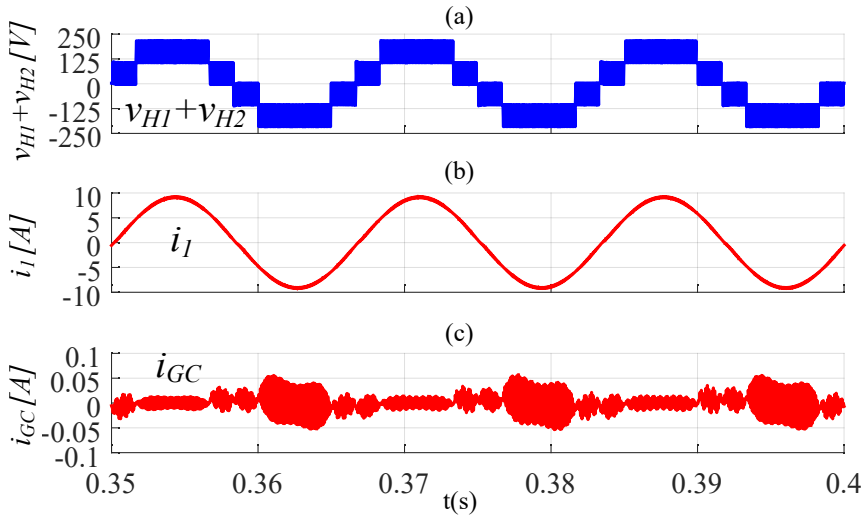

Fig. 4.25: IPD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

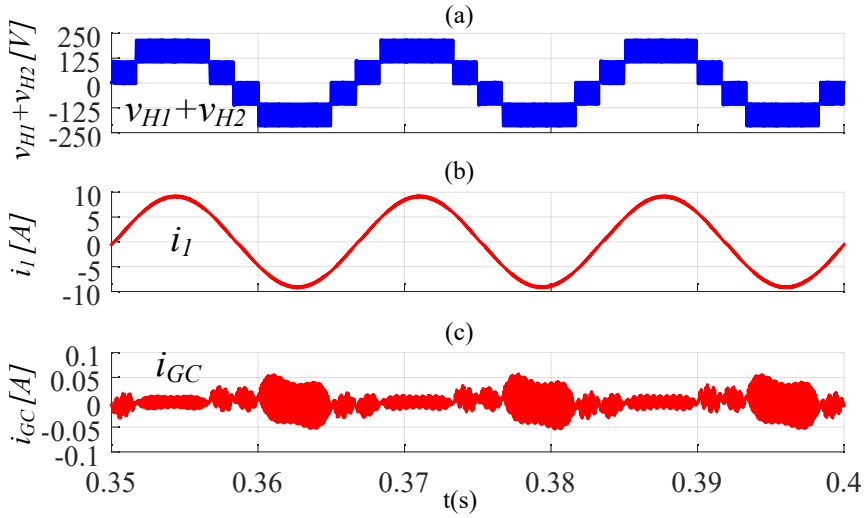

Fig. 4.26: POD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

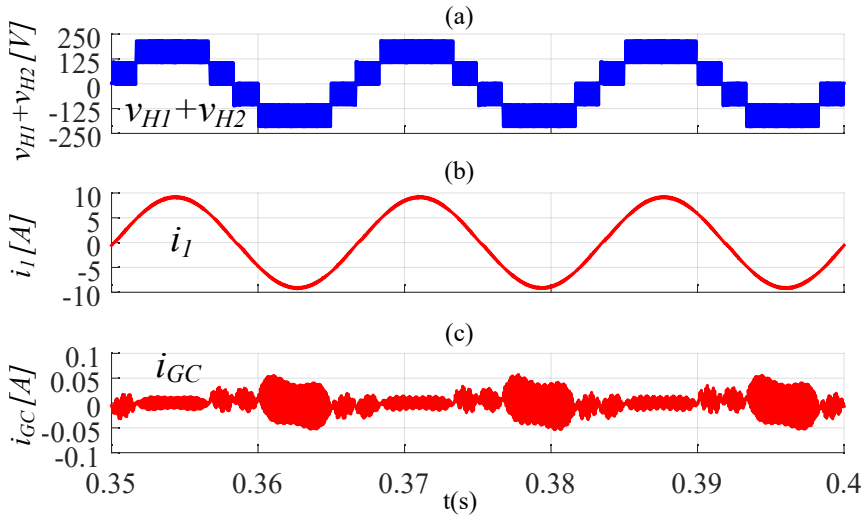

Fig. 4.27: APOD PWM: (a) output voltage ($v_{H1} + v_{H2}$), (b) grid current i_1 and (c) LGC i_{GC}.

5. EXPERIMENTAL VALIDATION

5.1 Experimental set-up

A $1\,\mathrm{kW}$ experimental prototype has been developed to perform the experimental tests of 5LCHB. Experimental prototype has been designed by means of IGBT power modules SKM75GB1200 and SKHI22A-R driver is used as a gate driver for each power module. An optical interface was implemented with the optical transmitter HFBR-1531Z and the optical receiver HFBR-2521, besides, a digital circuit is implemented to control the PWM, in this case the logic gate AND chip with open collector transistor SN75452B is used, finally a Digital Signal Processor TMS320F28335 is implemented in order to compute each PWM technique, the schematic for this section is illustrated in Fig. 5.1. Several output PWM signals from the DSP were connected to the module HFBR-1531z. Then, a enable/disable circuit is required to control the PWM signals. This characteristic is reached by a digital circuit as can be observed in Fig. 5.2. Notice that, the PWM signals can be started and stopped by different methods, that is, by optic signal as well as push button, in addition, there are different signals to enable the converter which are B7-Set, Set-soft, on the other hand, the circuit is disabled by a reset signal B8-Reset or Fault signal. The fault signal is an external signal which is transmitted by the converter in both optical and any control circuit by hardware.

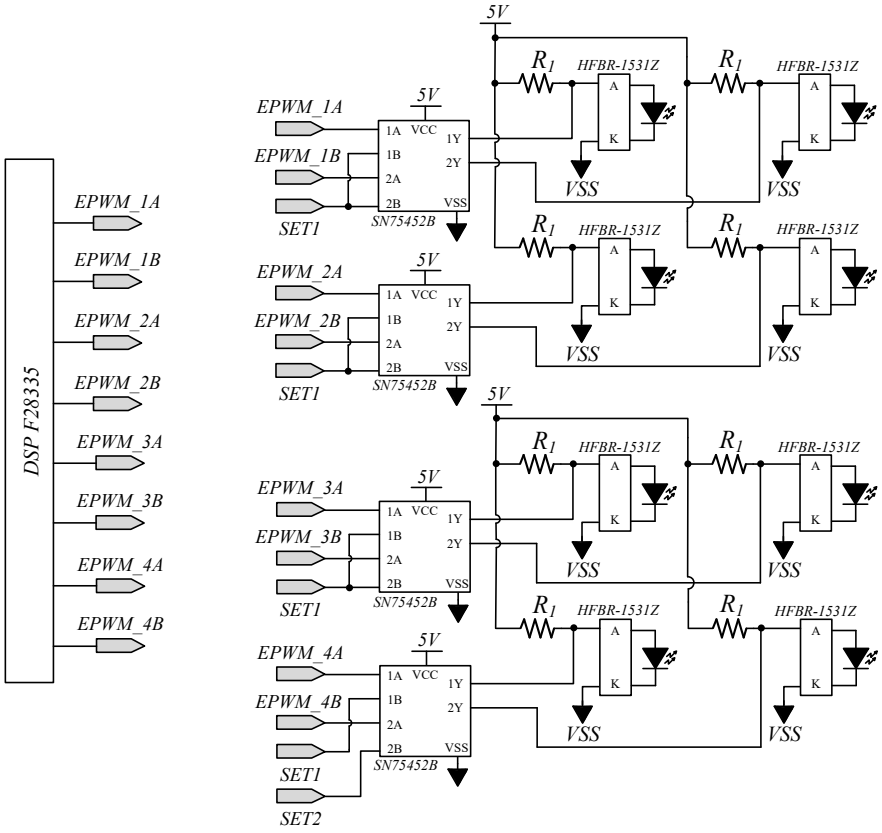

Fig. 5.1: Optical interface for PWM signals.

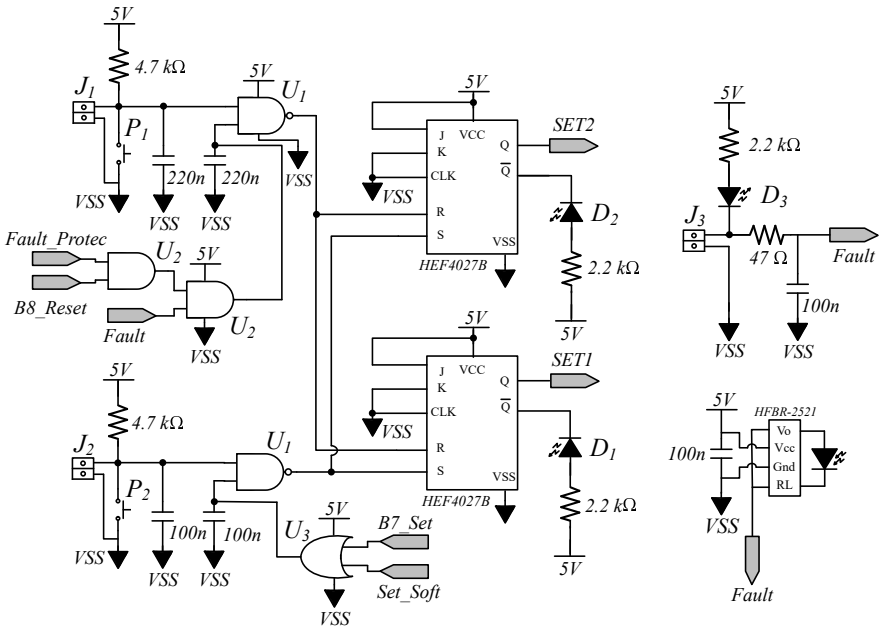

Fig. 5.2: PWM protection.

The power converter is switched by a IGBT gate driver, in Fig. 5.5 the schematic for the driver is shown. In this case, the PWM sequence is received by two fibre optic modules, then, the voltage is shifted to 15V since is the nominal voltage of the IGBT gate driver. In addition, the integrated circuit provides a fault signal which is used to design a enable/disable circuit within the PCB of the switching module, on the other hand, this fault signal can be transmitted to other gate driver modules, this characteristic allow to have many interconnected modules and obtaining a single fault signal which is detected by the DSP and turn off the converter by software. The experimental prototype of the DSP with the digital circuit for the PWM outputs and the IGBT module are illustrated in Fig. 5.3-5.4.

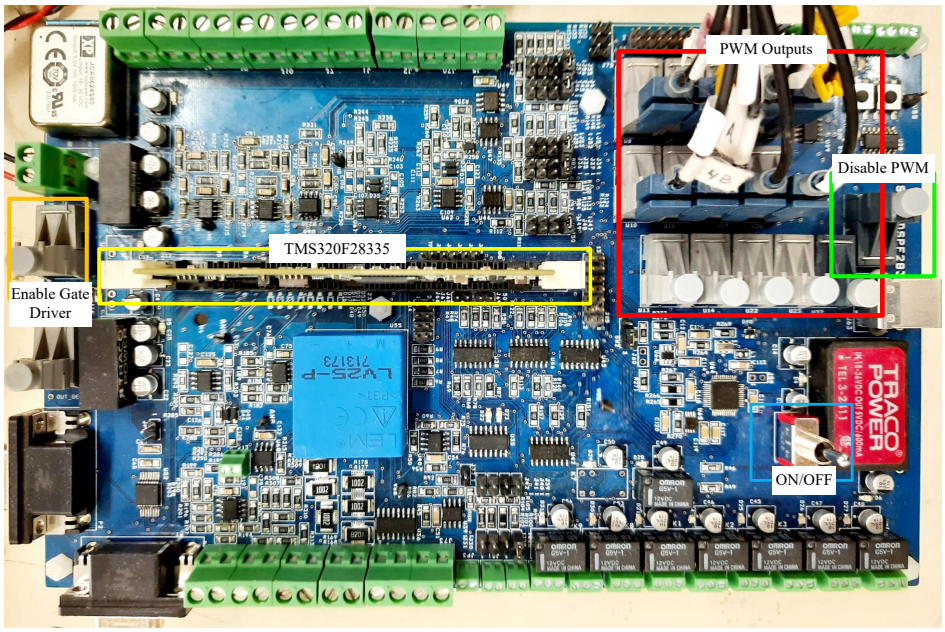

Fig. 5.3: Experimental prototype for DSP F28335.

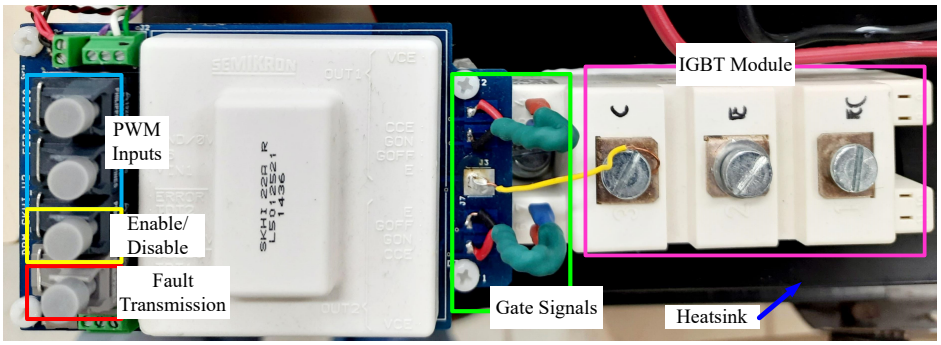

Fig. 5.4: Experimental prototype for IGBT module.

An electrical drawing for proposed converter is represented in Fig. 5.6. The experimental system set-up is depicted in Fig. 5.7. Stray capacitors are emulated by using four MKP capacitors connected to ground resistor in the leakage current path. The experimental prototype parameters are summarized in Table 5.1. Experimental results are presented in the following order: switching pattern for each PWM method, time response, frequency response and comparative analysis of the topology under study.

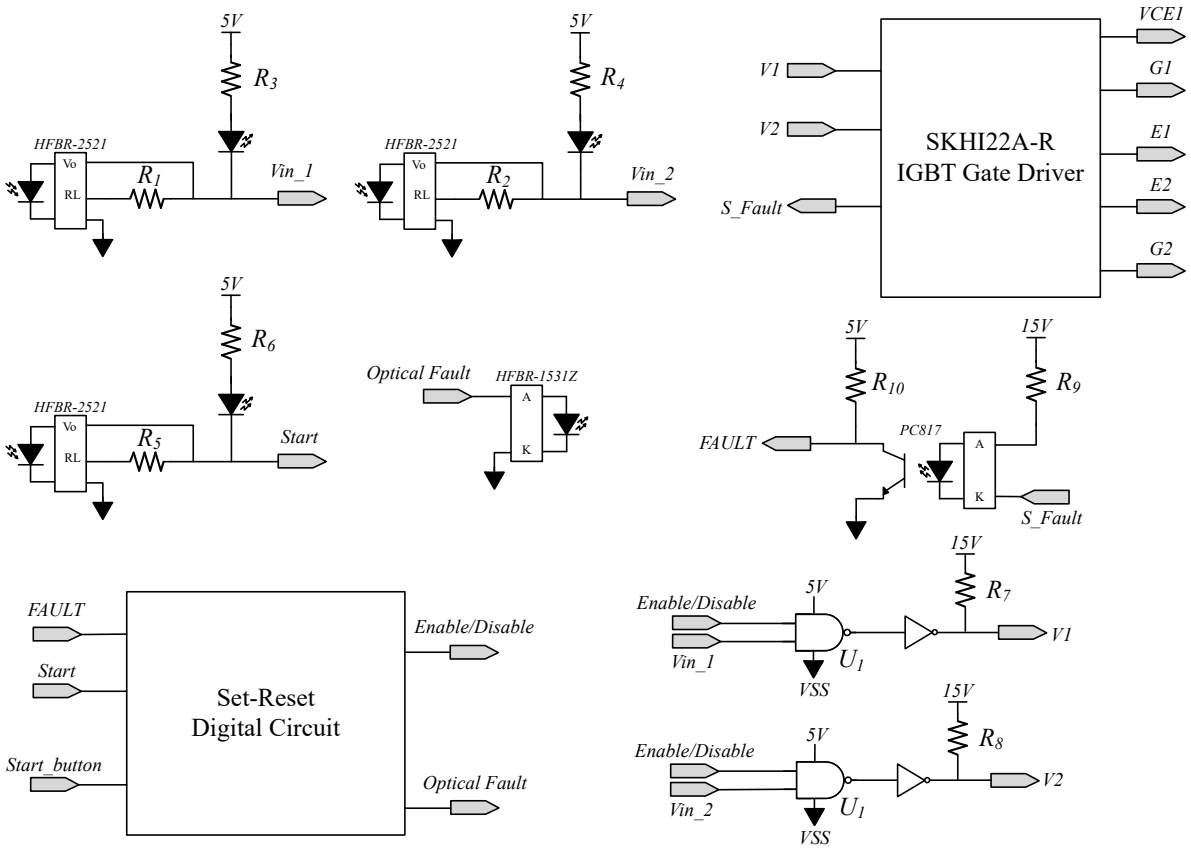

Fig. 5.5: Schematic for IGBT gate driver.

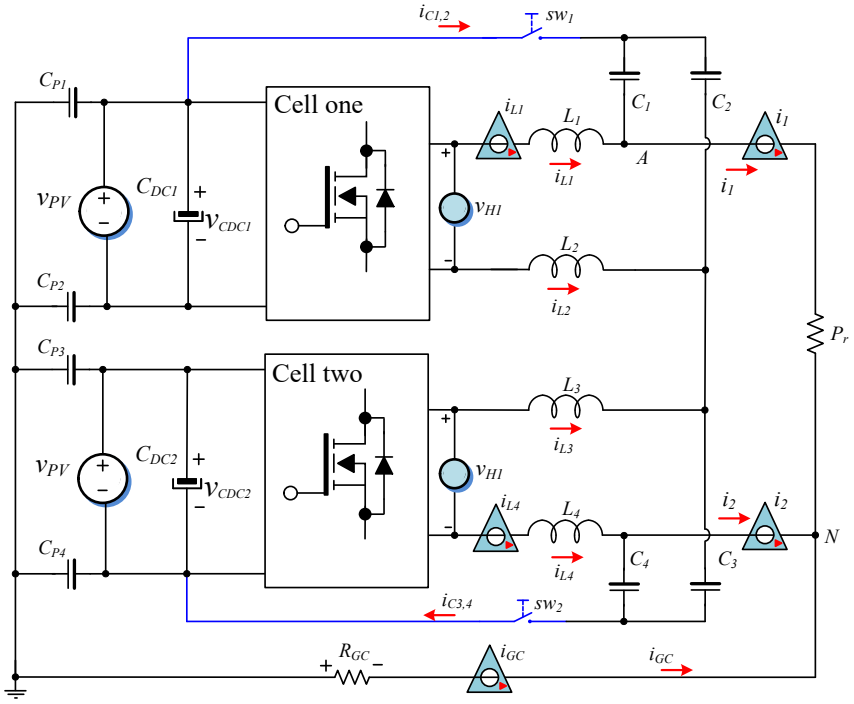

Fig. 5.6: Electrical drawing for experimental implementation.

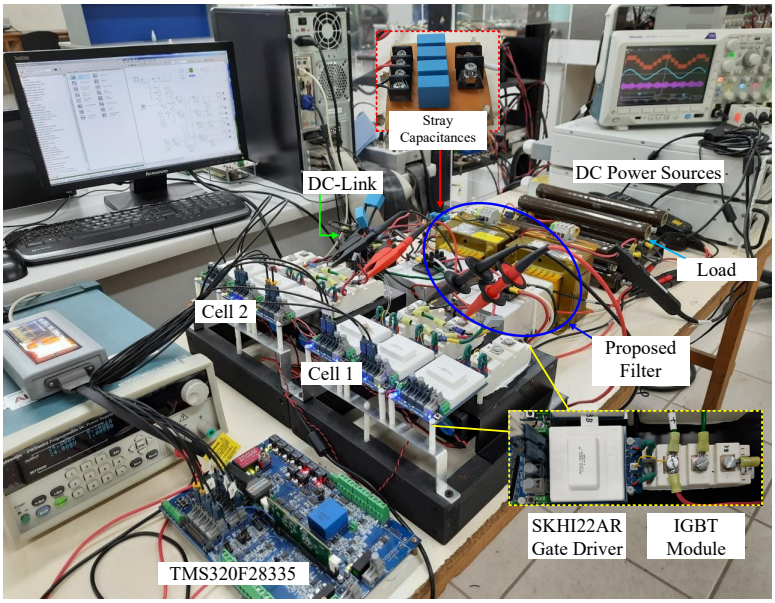

Fig. 5.7: Experimental prototype set-up.

Tab. 5.1: Prototype parameters.

Parameter	Value	Parameter	Value
v_{PV}	110 V_{DC}	C_{P1}, ..., C_{P4}	50 nF
C_{DC1}, C_{DC2}	2200 μF	R_{GC}	10 Ω
C_1, ..., C_4	5 μF	f_{sw}	10 kHz
L_1, ..., L_4	1 mH	f_g	60 Hz
P_r	20-50 Ω		

5.2 Experimental results

In this section, once the experimental prototype has been designed and implemented, the experimental results are presented and described. The gates signals for the modulation schemes IPD, POD and APOD are shown in Fig. 5.8, 5.9 and 5.10. It can be observed that the switching pattern is similar in these modulations. In addition, it is easy to show that the gate signals synthesize a five level voltage at the output.

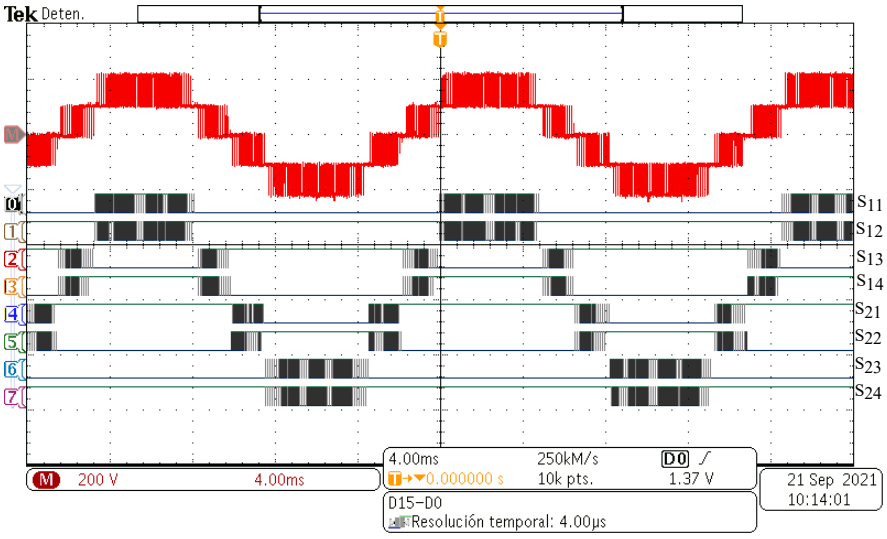

Fig. 5.8: From top to bottom (x-axis 4ms/div): output voltage (y-axis 200V/div) and gate signals for IPD PWM.

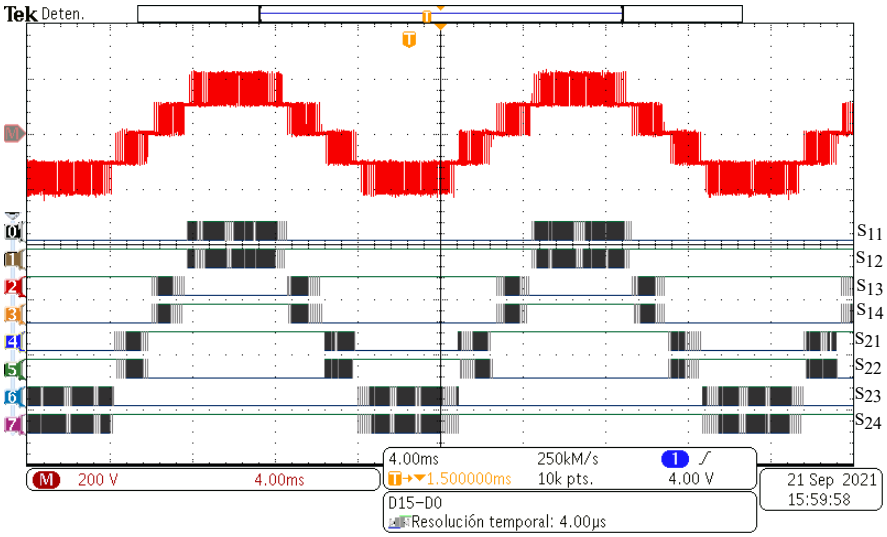

Fig. 5.9: From top to bottom (x-axis 4ms/div): output voltage (y-axis 200V/div) and gate signals for POD PWM.

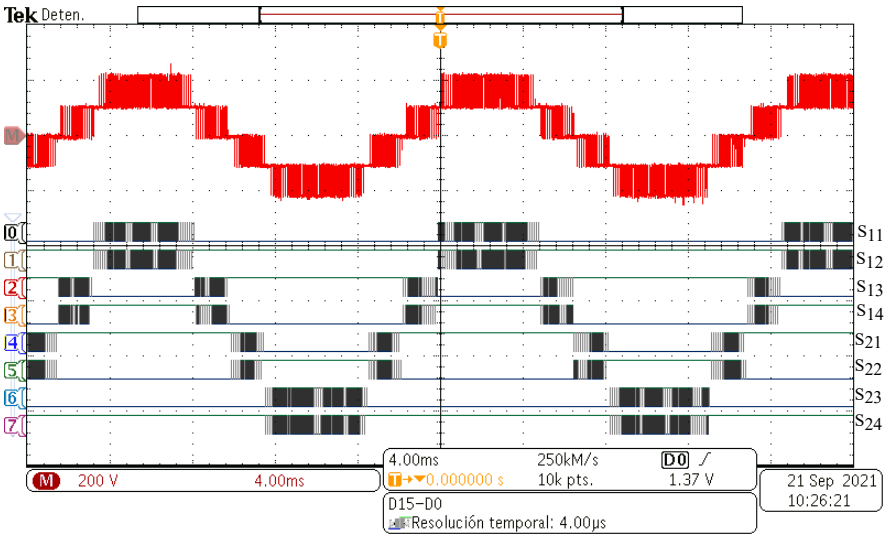

Fig. 5.10: From top to bottom (x-axis 4ms/div): output voltage (y-axis 200V/div) and gate signals for APOD PWM.

The PSPWM scheme obtained by experimental test is illustrated in Fig. 5.11. In this case, all power devices are always switching, and also a five level voltage waveform is achieved at the output.

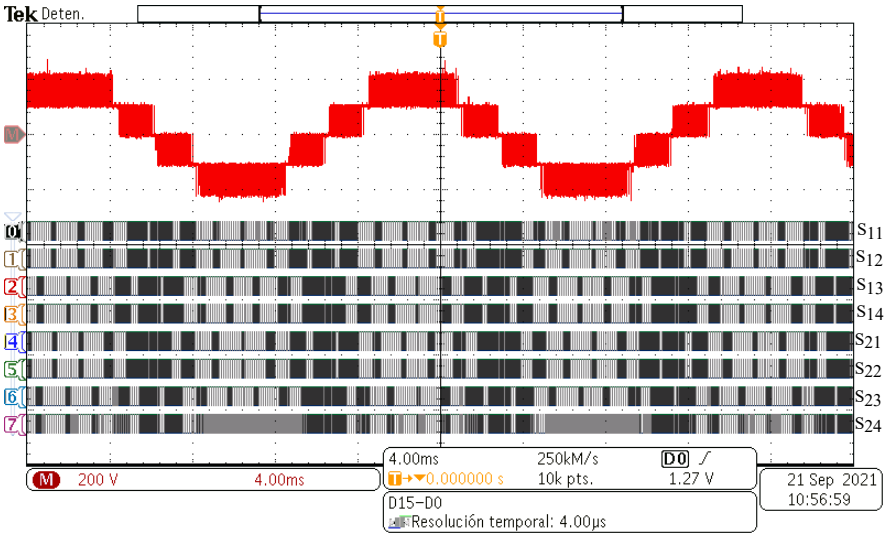

Fig. 5.11: From top to bottom (x-axis 4ms/div): output voltage (y-axis 200V/div) and gate signals for PSPWM.

Regarding to the LGC behavior in a 5LCHB topology, Fig. 5.12,5.13, 5.14 and 5.15 depict the steady state of the inverter output voltage, which is the sum of the cell one and two ($v_{\mathrm{H1}} + v_{\mathrm{H2}}$), grid current i_1 and LGC i_{GC}. As mentioned early, the i_{GC} waveform depends on the CMV variations, hence the i_{gc} waveform for the IPD, POD and APOD schemes is similar, where it reaches peaks closely to 1.2 A.

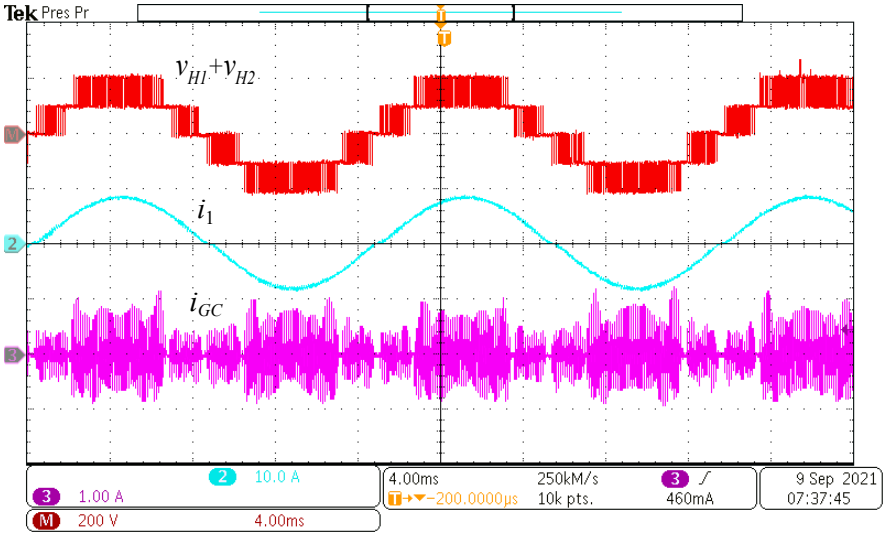

Fig. 5.12: Time response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 1A/div) for IPD.

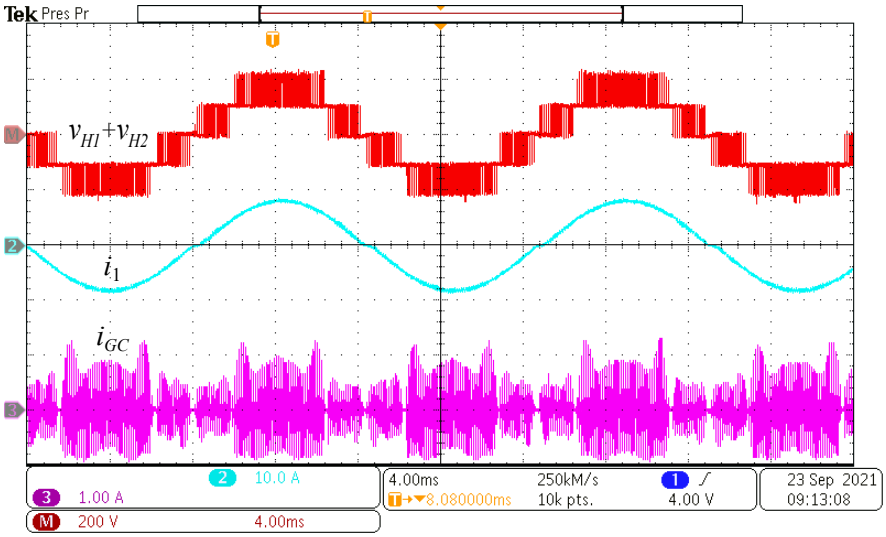

Fig. 5.13: Time response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 1A/div) for POD.

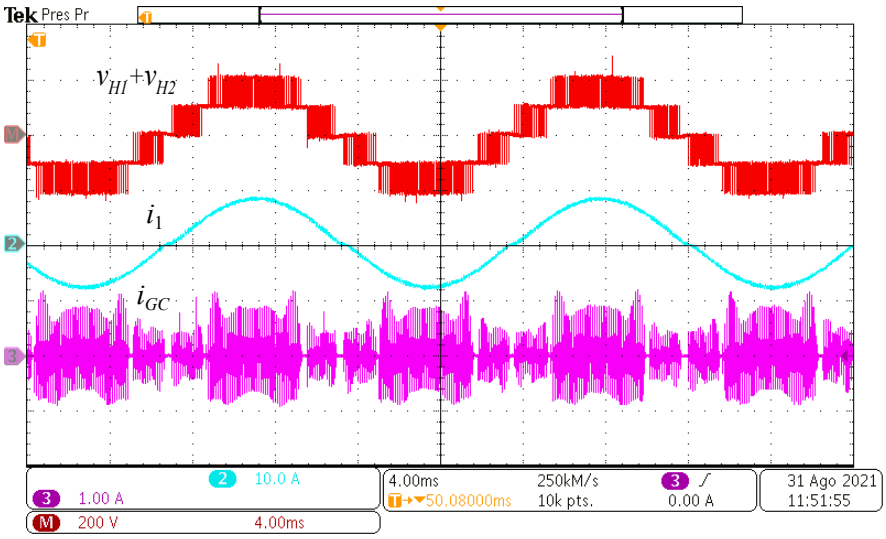

Fig. 5.14: Time response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 1A/div) for APOD.

Moreover, in the PSPWM modulation peaks around to 2 A have been reached in the i_{GC} and the waveform is different due to the switching of the power devices. However, the RMS values of i_{GC} are around 355, 338, and 364 mA for IPD, POD and APOD modulations, whereas the RMS value for PSPWM is 1.22 A, which are greater than 300 mA according to the standard DIN VDE 0126-1-1. In fact, a high leakage current value turns out in a distortion for the grid currents.

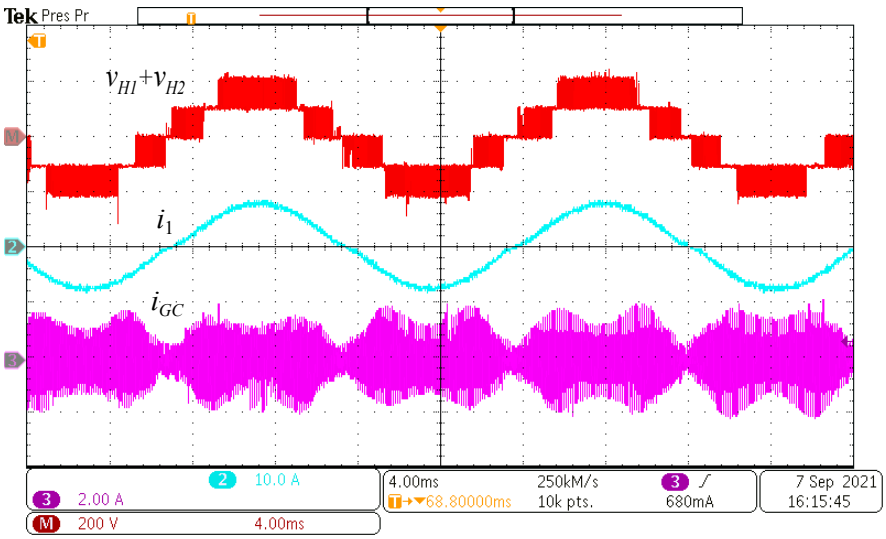

Fig. 5.15: Time response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 2A/div) for PSPWM.

The transient response of the proposed topology for leakage current behavior is performed by connecting and disconnecting C_1, C_2, C_3, C_4 by means of sw_1 and sw_2. In Fig. 5.16 the grid currents i_1, i_2 and i_{GC} are depicted for transient response analysis. Notice that, i_{GC} has been significantly reduced and as side effect the passive filter has a good performance regarding to filtering grid currents. Although, a distortion appears at zero-crossing, however it can be addressed by implementing a control loop. For POD and APOD techniques represented in Fig. 5.17 and Fig. 5.18, in these cases the same results are obtained compared with IPD scheme, that is, the LGC mitigation is achieved as well as filtering grid currents. In Fig. 5.19 the performance of PSPWM scheme is illustrated. It can be observed the effectiveness of the proposed filter in minimizing i_{GC} and also the high frequency components of i_{GC} present in the grid currents are filtered. As a result, after connecting the proposed filter in all PWM techniques under study, a high quality grid current waveform and a reduction of i_{GC} are obtained. In order to prevent the flow of i_{GC} to the electrical grid, the passive filter is connected. Nevertheless the filter operation forces the LGC to be recirculated through the converter and the CMC of the converter is increased, which may have a slightly effect in the overall efficiency.

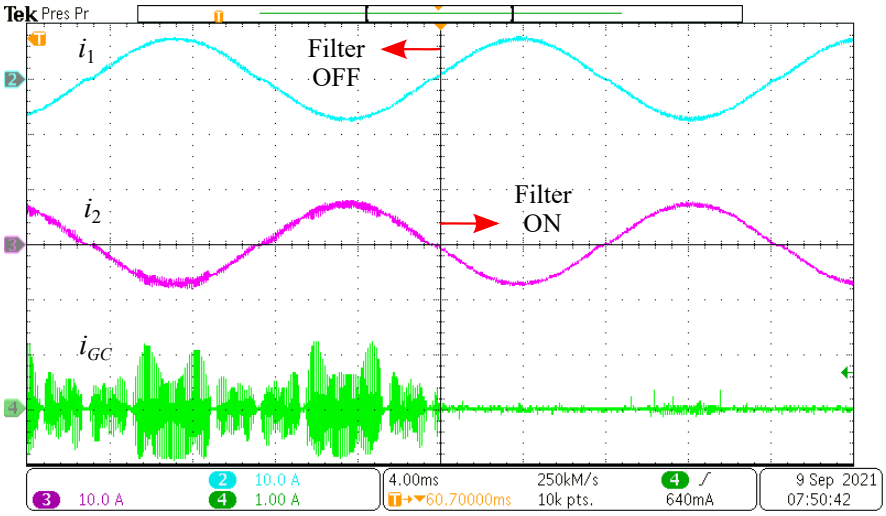

Fig. 5.16: Transient response (x-axis 4ms/div): grid currents (y-axis 10A/div) and ground current (y-axis 1A/div) for IPD before and after connecting filter.

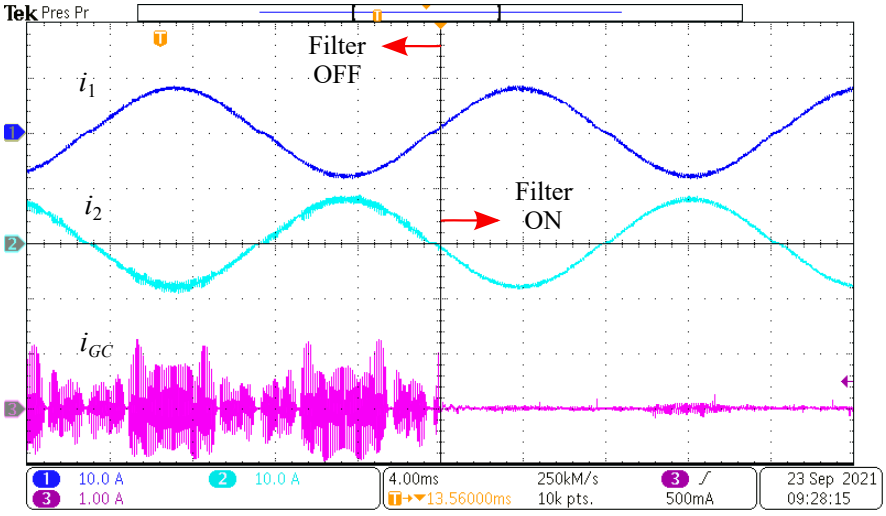

Fig. 5.17: Transient response (x-axis 4ms/div): grid currents (y-axis 10A/div) and ground current (y-axis 1A/div) for POD before and after connecting filter.

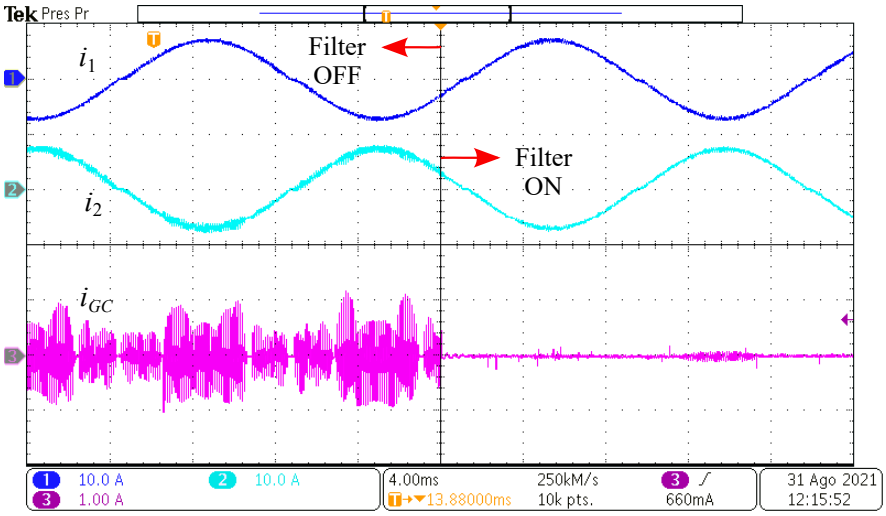

Fig. 5.18: Transient response (x-axis 4ms/div): grid currents (y-axis 10A/div) and ground current (y-axis 1A/div) for APOD before and after connecting filter.

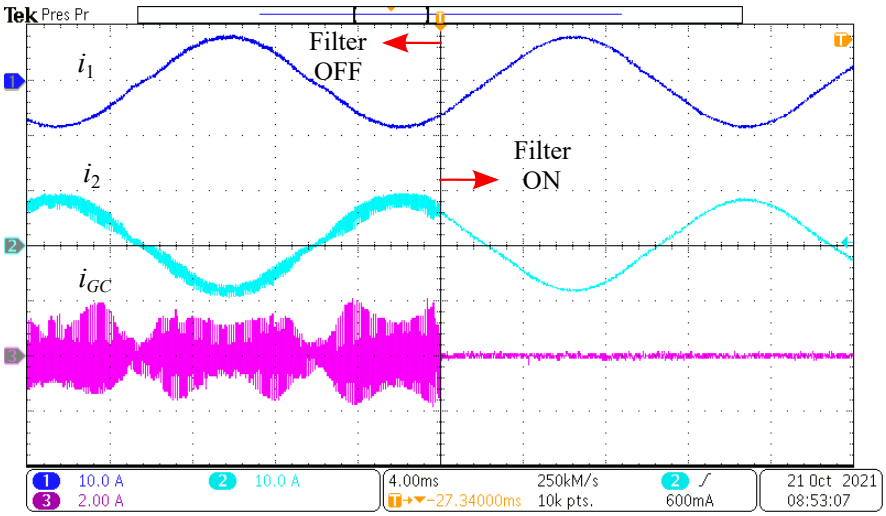

Fig. 5.19: Transient response (x-axis 4ms/div): grid currents (y-axis 10A/div) and ground current (y-axis 2A/div) for PSPWM before and after connecting filter.

In addition, the steady state response for PWM modulations applied to the 5LCHB with LC filter tied to DC-link are described below. Fig. 5.20 from top to bottom shows the output voltage ($v_{\mathrm{H1}} + v_{\mathrm{H2}}$), grid current i_1 and i_{GC}, notice that, the LGC is compensated. Although, a residual i_{GC} remains in the ground path, the RMS value of i_{GC} must be less than 300 mA and also a high quality current waveform is performed. Similar laboratory results are obtained for POD and APOD techniques. The results for the aforementioned PWM techniques are shown in Fig. 5.21

and 5.22. Fig. 5.23 depicts the steady state of the topology under study with PSPWM technique. The magnitude of LGC has already been effectively suppressed and grid current i_1 is filtered.

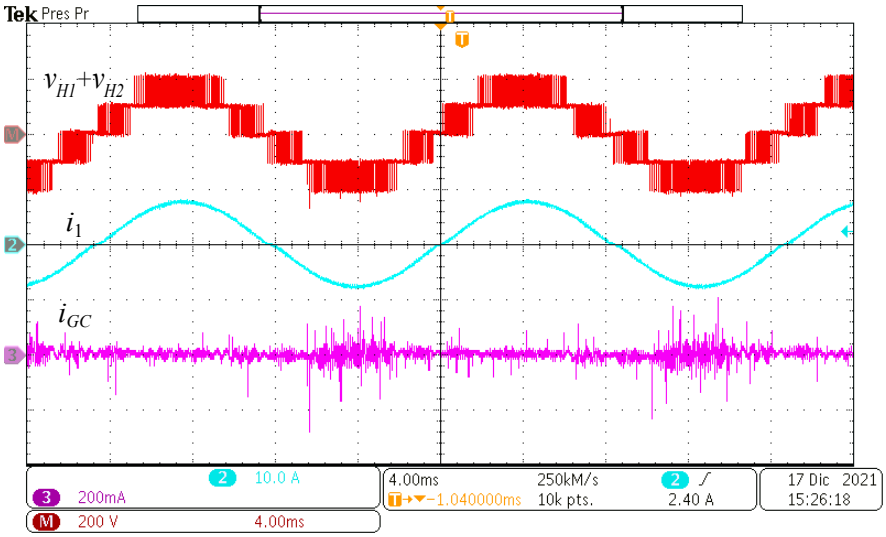

Fig. 5.20: Steady-state response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 200mA/div) for IPD with LC filter.

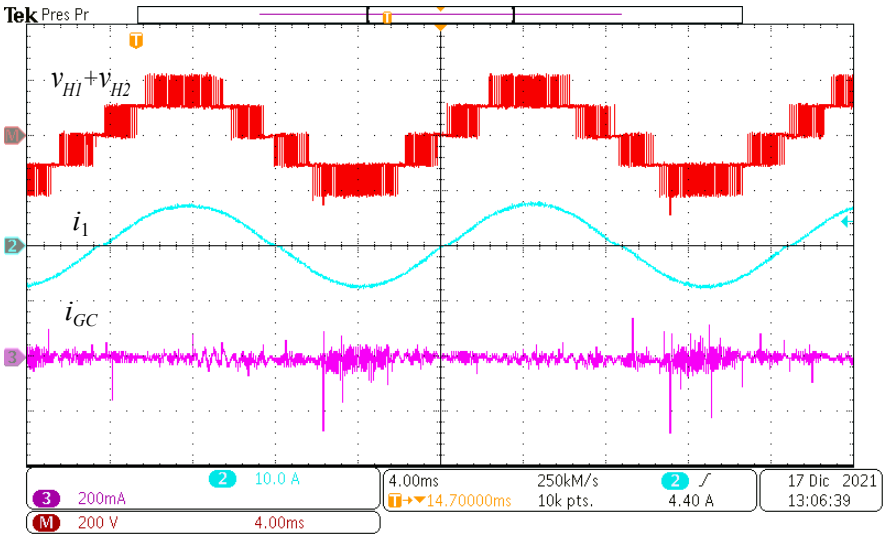

Fig. 5.21: Steady-state response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 200mA/div) for POD with LC filter.

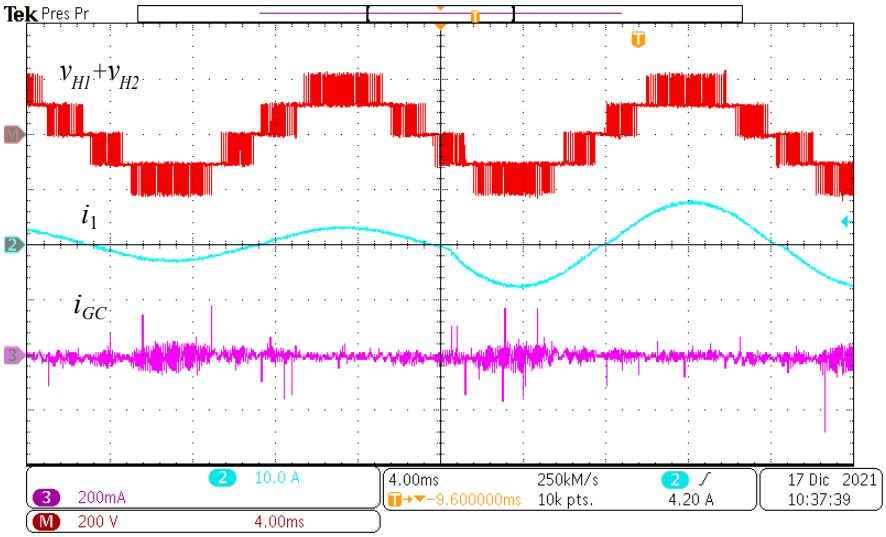

Fig. 5.22: Steady-state response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 200mA/div) for APOD with LC filter.

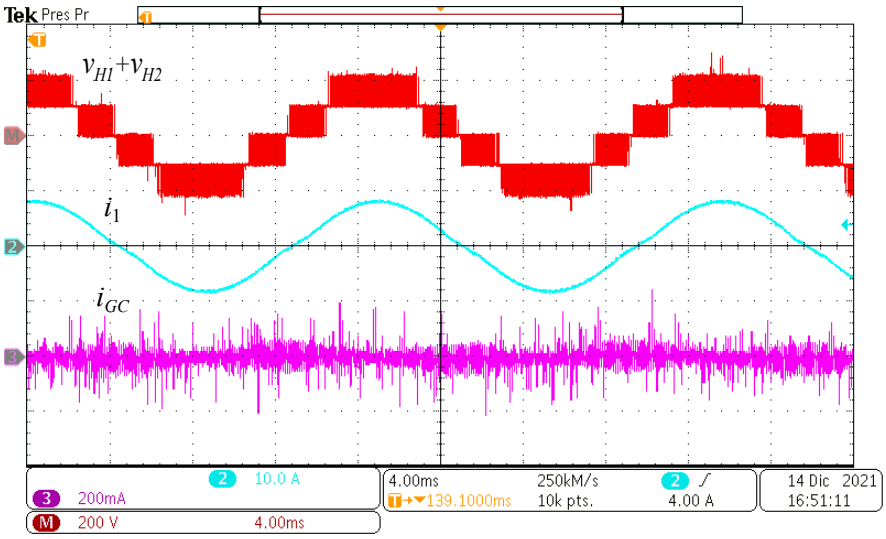

Fig. 5.23: Steady-state response (x-axis 4ms/div): output voltage (y-axis 200V/div), grid current (y-axis 10A/div) and ground current (y-axis 200mA/div) for PSPWM with LC filter.

Frequency response of the studied converter and also the passive filter is described bellow. As it is expected, the frequency response for level-shifted PWM methods is very similar as can be observed in Fig 5.24, 5.25 and 5.26. The harmonic content for these PWM methods are compensated and it is easy to observe that the THD for i_o is within of the requirements for power injection according to the IEEE 519. In addition, the dominant harmonics of $V_{H1} + V_{H2}$ appear as a side-band, around m_f, which is defined as $m_f = f_{sw}/f_g$. On the other hand, for

PSPWM method the dominant harmonics appear as a side-band centered around $4m_f$ and as a result the THD of the inverter output voltage is less applying the PSPWM techinque to 5LCHB than level-shifted methods.

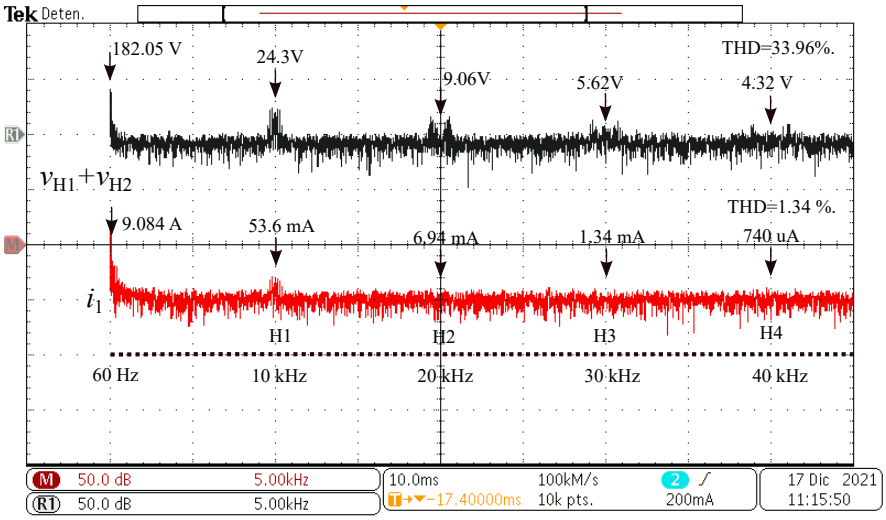

Fig. 5.24: Frequency response (x-axis 5kHz/div): FFT Output voltage (y-axis 50dB/div) and grid current (y-axis 50dB/div) for IPD with LC filter.

In order to estimate the THD of the IPD PWM harmonic distribution the Fig. 5.24 is considered. From top to bottom the Fast Fourier Transform (FFT) is depicted for $v_{H1} + v_{H2}$ and i_1, and the calculated THD obtained is 33.96% and 1.34% respectively.

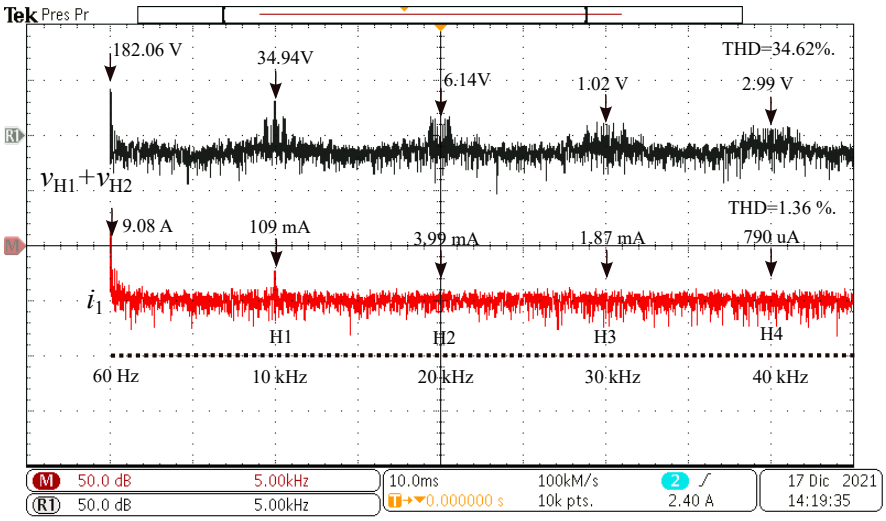

Fig. 5.25: Frequency response (x-axis 5kHz/div): FFT Output voltage (y-axis 50dB/div) and grid current (y-axis 50dB/div) for POD with LC filter.

From the Fig. 5.25 the THD for POD technique is calculated. Notice that, the harmonic content is different regarding IPD PWM, in this case there are more side-band around the dominant harmonic which indicates that the THD will be affected. The THD for the output voltage and grid current are 34.62% and 1.36%.

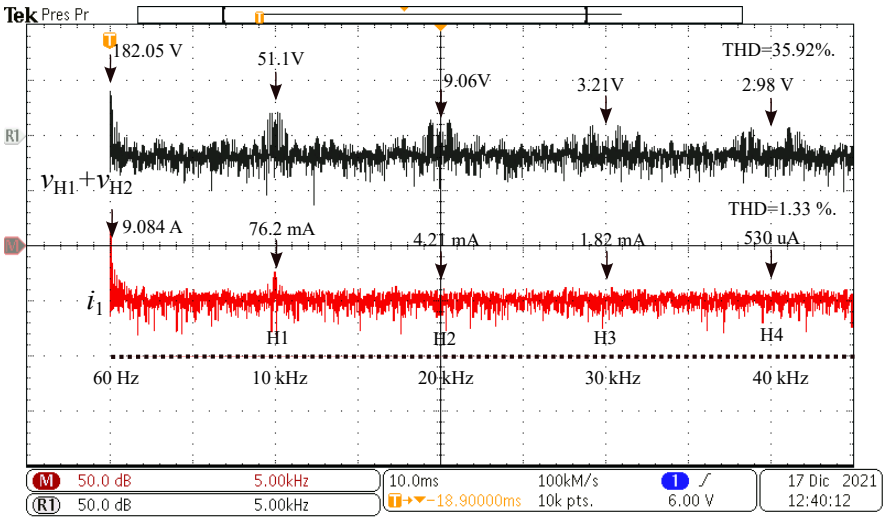

Fig. 5.26: Frequency response (x-axis 5kHz/div): FFT Output voltage (y-axis 50dB/div), grid current (y-axis 50dB/div) for APOD with LC filter.

The FFT for APOD technique is illustrated in Fig. 5.26, it is easy to observe that the harmonic distribution has many side-bands around the dominant harmonic, the voltage THD is affected since these side-bands, as a result of the FFT the voltage and current grid THD estimated are 35.96% and 1.33% respectively. As it was expected, the first harmonic $H1$ for the LSPWM methods appears at 10 kHz since the effective frequency of these PWM sequences are equal to the switching frequency.

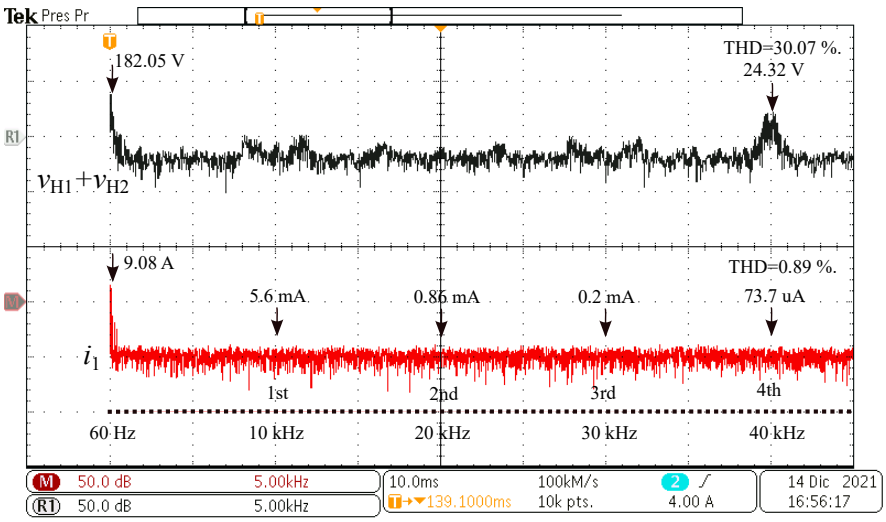

Fig. 5.27: Frequency response (x-axis 5kHz/div): FFT Output voltage (y-axis 50dB/div), grid current (y-axis 50dB/div) for PSPWM with LC filter.

The remarkable advantages of the PSPWM method regarding to harmonic distribution is shown in Fig. 5.27. This method displaced the voltage harmonics until $4f_{sw}$, that is, the first harmonic appears around 40 kHz. So that, the voltage and current THD are estimate according to the Fig. 5.27 and 30.7% for the voltage THD, whereas the current THD is 0.89%. A summary of the results in this thesis are listed in Table 5.2 which considers as key parameters both the output voltage and grid current, THD, ($THD_{v_{H1}+v_{H2}}$, THD_{i_1}) as well as the inverter frequency or the effective frequency of each PWM method, the LGC magnitude before and after the filter connection (L and LC Filter), the current ripple of i_1 and the efficiencies η_{EURO} and η_{CEC}. Ac-

Tab. 5.2: Summary results of the proposed structure.

PWM method	$THD_{e_{DM}}$	THD_{i_1}	i_{GC}(RMS) Filter (L)	i_{GC}(RMS) Filter (LC)	$f_{s,inv}$	η_{EURO}	η_{CEC}	$i_{1(ripple)}$
PS PWM	30.07%	0.89%	1.22 A	29.3 mA	40 kHz	92.17%	93.67%	19.89 mA
IPD	33.96%	1.34%	355 mA	18.7 mA	10 kHz	95.3%	96.51%	264.10 mA
POD	34.62%	1.36%	338 mA	21.6 mA	10 kHz	95.3%	96.51%	264.11 mA
APOD	35.92%	1.33%	364 mA	20.6 mA	10 kHz	95.3%	96.5%	264.11 mA

cording to Table 5.2 the proposed filter which is implemented in a CHB topology is an excellent alternative to suppress the LGC in transformer-less systems. The experimental results turned out

in a very low LGC magnitude as well as a good performance regarding THD. The PWM methods have been assessed and as consequence the LGC mitigation is allowed without depending on the switching pattern of the PWM technique. In other matters, the RMS LGC magnitude of the PSPWM with the second order filter is greater than the level-shifted methods since in this technique the LGC contribution due to the switching scheme is much higher. Therefore, the standard DIN VDE 0126-1-1 is accomplished. Furthermore, it is easy to observe that the effective frequency of the PSPWM technique when the filter is connected turns out in an improvement in terms of harmonic attenuation. Comparing the results in terms of THD for each PWM method with the proposed second order filter, the PSPWM is better than the LSPWM method regarding the results obtained without LGC compensation method shown in Fig. 4.2. This feature of the PSPWM allows the inverter to be operated at a lower frequency without significant side effects on the THD parameter.

6. CONCLUSIONS.

In this research project an analysis of a CHB converter with LC filter is presented. The inclusion of the particular connection of the LC filter allowed to mitigate the LGC. As it is observed in chapter 3, the mathematical analysis of the proposed filter with the CHB converter turned out in the differential and common mode models. Using the model expressions of the CMM an electric circuit can be drawn and taking into consideration the CMM circuit the LGC behavior is explained. As a result of the LC filter connection a new path for the LGC is created. Notice that, the capacitor of the filter provides a low impedance trajectory where LGC can flow and avoid the injection of the high-frequency harmonics into the utility grid. In addition, the filter design procedure was based on DMM and the switching frequency was obtained by the polynomial characteristic of the transfer function $G_{DM}(s)$. Then, L and C values for the proposed filter are based on several considerations of the prototype parameters. Regarding to the steady-state response, for LSPWM methods the LGC waveform remains a peak around $200\ \mathrm{mA}$ in the negative semicyle since there is a low frequency variation of the CMV as observed in the Fig. 4.21-4.23. On the other hand, the LGC waveform for the PSPWM is always varying along the grid period since the CMV in this method is a low frequency sinusoidal waveform, however, the LGC peak value is less than $200\ \mathrm{mA}$. According to the results the LGC RMS value for each PWM technique under study are 18.7 mA, 21.6 mA and 20.6 mA for IPD, POD and APOD respectively, on the other hand, the highest LGC value is for PSPWM with 29.3 mA. The transient response is evaluated through a power change between $400\ \mathrm{W} - 900\ \mathrm{kW}$, as a result of these experimental tests it is observed that the behavior of the LGC is not affected since the LGC magnitude is kept for all PWM schemes under study. In other matters, the efficiency for level-shifted methods is better that PSPWM method with a value around 96%, meanwhile, for PSPWM method is around 94%. Therefore, the proposed LC filter for a CHB converter turns out in a suitable structure for single-phase transformerless photovoltaic applications due to the LGC RMS value is less than

300 mA which is the value established by the international regulations.

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